The SOL-20 Computer's Cassette interface.

(H. Holden. Dec. 2018)

Introduction:

The Cassette interface designed by Processor Technology (PT) for their SOL-20 was made to be compatible with the Kansas City format (300 Baud system) as well as a 1200 Baud system, the default system in the Sol-20 called CUTS. So there was an effort in PT's design to use a known pre-existing standard, even though it is not the default. Cassette tapes sold by PT, such as BASIC/5 for example, had the 300 Baud recording on one side of the tape and the 1200 Baud recording on the other.

These recordings are "Two Tone" systems, where two different audio frequencies represent logic 0 and logic 1.

PT's CUTS uses a 1200 Hz and a 600 Hz tone, while Kansas City format uses a 2400 Hz and a 1200 Hz tone. The official title for this modulation system is called AFSK, or audio frequency shift keying.

In both the 300 Baud and 1200 Baud systems, the UART's serial data is configured as one start bit, 8 data bits and two stop bits. In the 300 Baud system, the time period that the serial output data from the UART is high or low allows some number of cycles of each of the two audio tones to be outputted or recorded. In the case of the 300 Baud Kansas City format, 8 cycles of 2400 Hz represent a "1" and 4 cycles of 1200 Hz represents an "0". Therefore a bit has a length or duration of 3.33 mS of the audio tone. In PT's 1200 Baud system, a bit occupies a length of 1 cycle of 1200 Hz, or half a cycle of 600 Hz, or 0.833mS.

The thing that struck me about the above, is that in PT's 1200 Baud system, the tone decoder circuitry, processing the data from a played back tape, would have to be able to identify the 600 Hz tone from only one half cycle of it in the audio stream, compared to the Kansas City format where there are a minimum of 4 cycles of tone to process or identify. It turns out of course that PT's clever tone decoder only requires ½ a cycle of the 600Hz tone to identify it quickly.

The binary serial data stream, for recording a tape, originates from the serial output of a standard UART IC, the TMS6011.This binary data is used to switch between the two tones to be recorded.

On the other hand, in the playback of a tape, the recovered tones are decoded into binary logic 1 and logic 0 data and sent to the UART's input. This idea greatly simplified

the interface, as ultimately the bytes comprising the program or file are read into, or out of memory, via the UART, just as they would be on a standard RS-232 serial link. This is also why the SOL-20 computer contains two UART IC's, one is used for the usual RS-232 serial interface, the other for the tape I/O.

PT's Solos operating system arranges it so that each cassette recording contains a header file with the file name and the beginning and ending address of where the program is loaded to memory. The program can be downloaded to memory from the tape with the GET command or downloaded and executed with the XEQ command. Also the ability to read a tape and show what programs are present on it is provided with the CAT command, which is very helpful. The selection of the 300 Baud standard is also under software control with the SET TAPE 1 command.

The purpose of this article is to examine the circuitry (hardware) in the Audio Tape I/O area of the SOL-20 motherboard (not the software). Hopefully this information could be useful in servicing or fault finding, if this part of the computer was found to be faulty.

Although the SOL-20 hardware manual is generally good, there is the occasional error and it is always helpful to have extra information or another view on how the circuit works.

Cassette Interface Circuitry:

Before looking at the actual arrangement of the cassette interface circuitry and how it works, it is worthwhile looking at a diagram of the origin of the timing pulses that control it. These come from the Baud Rate generator. The diagram shows the locations of these pulses making it quick & easy to see if they are “present and accounted for” with the scope or frequency counter:

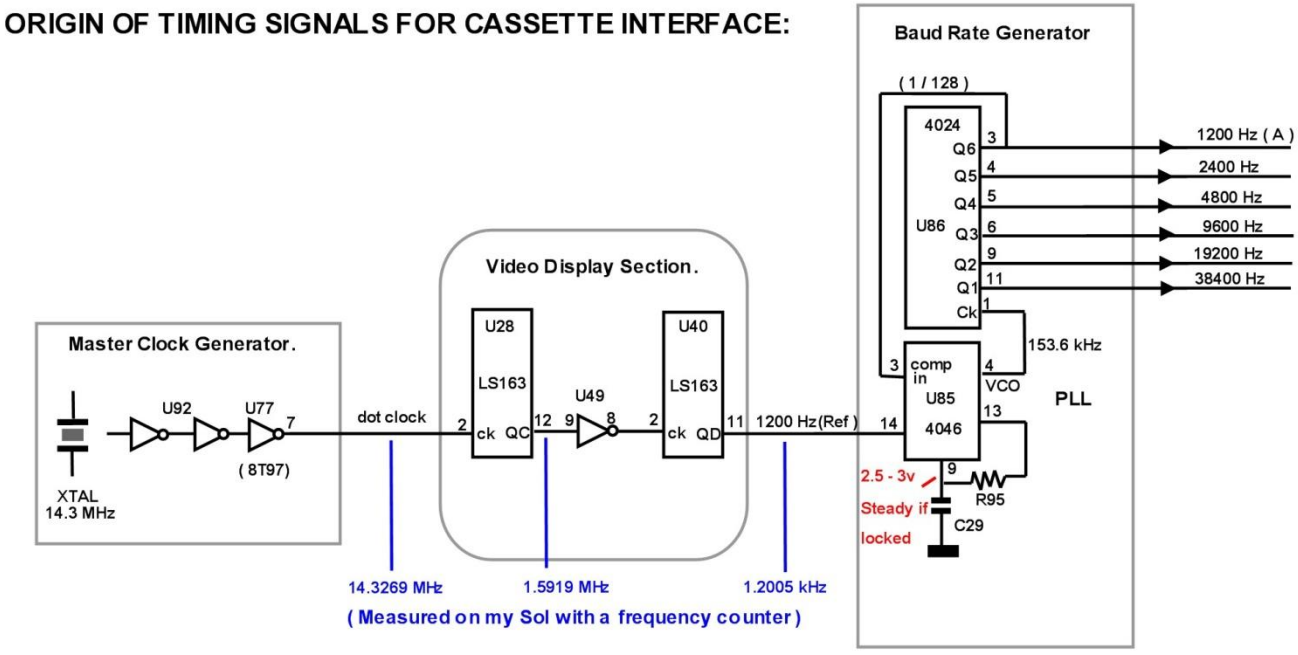


Fig. 1

The master clock measured at 14.3269MHz in my SOL with a frequency counter. It might be a little different on other Sols depending on the exact crystal and the calibration of the frequency counter, but it should be close to 14.3MHz.

As shown in figure 1, the Baud rate control pulses are derived from a PLL circuit locked to a x128 multiple of the 1200 Hz (ref) signal, which was derived from the computer’s divided down master clock.

If the PLL (U85) is in lock and working properly the DC feedback control voltage for the VCO on pin 9 will be *steady* in the range of 2.5 to 3 volts or thereabouts.

Generating the “two tone” pulses for recording:

CUTS (the1200 Baud mode) corresponds to a “TAPE HIGH SPEED” control signal being logic 1 and it is the default state, or the state specified with the command SET TAPE 0. In this case the two output frequencies recorded corresponding to a 1 and 0 of the UART’s output data stream, are 1200Hz and 600Hz.

If SET TAPE 1 is specified to change the Baud rate to 300 for the Kansa City standard, it alters the two recorded frequencies, making them 2400 Hz and 1200Hz tones. In the diagram of figure 2 below, these altered frequencies are shown in green for the 300 Baud mode.

The control signals that specify the two Baud rate modes are derived from an output register (Tape control latch port U97) on the data bus and are labelled TAPE HIGH SPEED, which is normally logic 1 for CUTS and its complimentary logic level, /TAPE HIGH SPEED is normally logic 0.

The SET TAPE 1 command in Solos, which specifies the 300 Baud rate, is only active during either loading a tape to the computer, or writing to a tape. The logic levels of TAPE HIGH SPEED and /TAPE HIGH SPEED revert to the 1200 Baud arrangement at other times, even if SET TAPE 1 has been specified by the user. Therefore, in an idling state, 1200 Hz is seen at the audio output jack, not 2400 Hz, even if SET TAPE 1 has been specified. The 2400Hz signal is only ever seen at the tape signal jacks in the process of reading a 300 Baud tape or recording a 300 Baud tape. Also, if the CPU is reset, the default state of 1200 Baud is set, equivalent to re-entering the command SET TAPE 0.

This means that to load a tape successfully, the user has to know if it was recorded as a 300 Baud or 1200 Baud format. At least if that was initially unknown, then listening to the payback signal from the tape would reveal the higher frequency tones of the 300 Baud system.

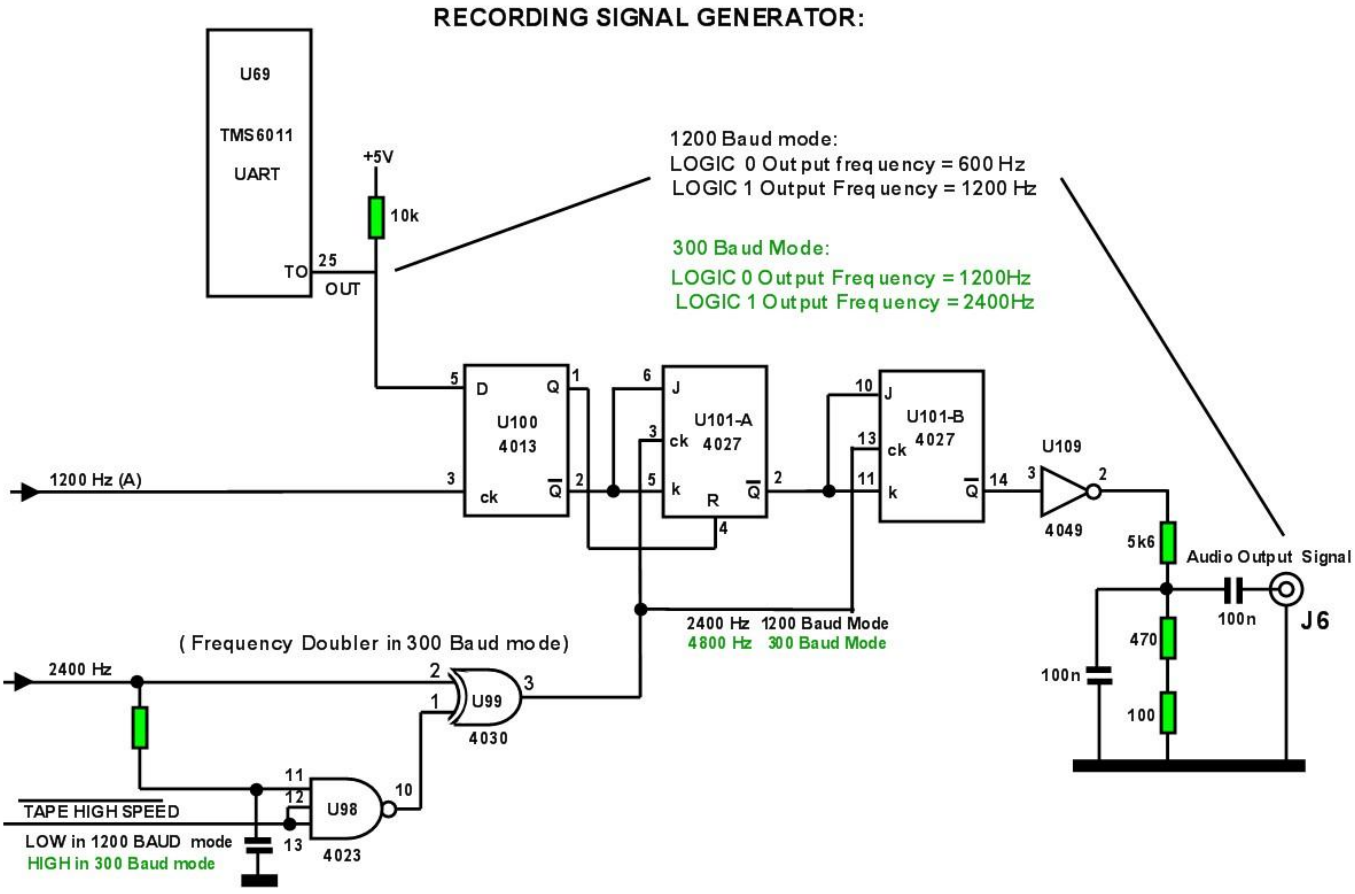


Fig. 2A

Record Circuit Operation:

As shown in figure 2A above, the 1200 Hz (A) signal from the Baud rate generator continuously clocks the serial data from the output of the TMS6011 UART IC to the Q and /Q outputs of U100. For the purpose of this discussion the halves of U101 are labelled as A and B.

In the case that the UART data is logic1, then pin 2 of U100 remains low as do the J & K inputs of U101-A. In this case U101-A not only is unable to toggle but also is kept in a rest mode by the logic 1 (Q output of U100) being applied to pin 4. This results in logic 1 on the /Q output of U101A being applied to the J &K inputs of U101B. With both the J&K high, a J-K flip flop becomes a very reliable toggling flip flop. As a result U101-B is toggled by the clock pulse on its pin 13. In the 1200 Baud mode this clock pulse is 2400Hz, therefore a 1200 Hz tone appears at the audio output.

In the case of 300 Baud mode, the clock pulse for U101- A & B is 4800 Hz, so 2400 Hz appears at the audio output, when there is a logic 1 at the UART's output. This mode is selected by a high logic level at U98 pin12 & 13. The Nand gate U98 delays one input of

the XOR gate's inputs and U99's output, pin 3, doubles in frequency as it responds to *both* the high & low transitions of the 2400 Hz input signal on pin 2 ofU99.

On the other hand, if the output of the UART is logic 0, more interesting things happen:

U101-A is released from reset, also its J&K inputs are now logic 1 as a result of the /Q output of U100 being high, so now U101-A is able to toggle on clock pulses.

The result is a 1200 Hz square wave (1200 Baud mode) being applied to the J & K inputs of U101-B. Since U101-B can only respond to a clock pulse, by toggling, when its J&K inputs are logic 1, it only responds every 2nd clock pulse.

Since U101-B only responds to every second clock pulse and U101-B itself divides by two, the output frequency of U101-B is now 2400/4 or 600Hz.

In summary, U101-A and U101-B are a divide by 4 synchronously clocked counter, converted into a divide by 2 counter when U101-A is disabled by U100, which is controlled by the UART data. The net result, in the 1200 Baud mode is that a logic 1 output from the UART results in a 1200 Hz tone, and a logic 0 generates a 600 Hz tone. (In the 300 Baud mode, both these tone frequencies are doubled).

Of note: for a single bit, representing logic 0 from the UART, only ½ a cycle of the 600 Hz tone is recorded because the UART output is only low for 0.833 mS.

The ½ cycle of recorded audio tone though is not necessarily low, it can be low or high, see below. Also, there is some RC filtering of the output signal which rounds off the square form of the waves (higher frequency harmonics) to be recorded by the tape deck.

The diagram below of figure 2B, shows the relationships of the pulses when the bit stream from the UART is 1 0 11. The rising edge of the 1200 Hz(A) pulse clocks the UART's output to the outputs of U100, about 1/2 the way into the length of the pulse to enable U101-A to count converting the counter comprised of U101 A & B to divide by 4. But due to the short time the UART output is low (0.833mS) for a logic 0, only one transition of the 1200 Hz output is missed:

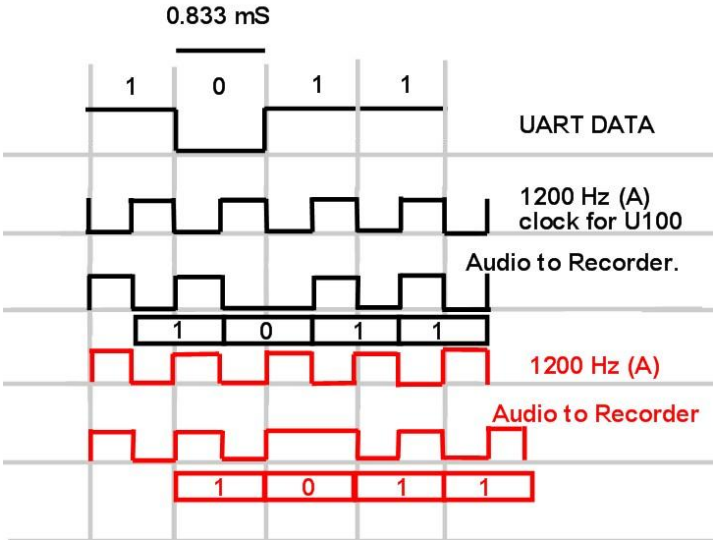


Fig. 2B

It turns out though that there is more to this transmitting circuitry than meets the eye. I noticed while I was looking at the timing relationships of the pulses around U100 and U101 A & B, I was getting some different measurement results at times.

Shown in red in figure 2B is one variation that can occur when the phase relationship of the output pulse from the UART has a ½ cycle difference with respect to the 1200 Hz (A) clock, even though the UART is ultimately being clocked, in transmit mode, by the same signal source from the Baud rate generator. Looking at the Baud rate generator design, any of the pulses derived from the 4024 ripple counter (U86 in Figure 1) could have reversed phase with respect to each other because there are no power up resets are applied to the counter, or resets at other times and it is a matter of chance often what state the flip flops in the 4024 come up in, at power up, even if they have a disposition to come up in one state or another. In transmit, the UART is clocked by the 19200 Hz pulse, and the tape output circuit by the 1200 Hz(A) and 2400 Hz pulses, which have no guaranteed phase relation between them.

Also, although U101-A is subjected to resets, U101-B which provides the tape audio output signal is not. At power up the Q and /Q outputs come up randomly (but still complimentary). Therefore the audio output pulses can also be inverted compared to what is shown in figure 2B. This gives a number of possibilities for the exact appearance (timing and polarity) of the audio output pulses with respect to the UART's pulses, looking with a dual channel scope.

In all cases though, the serial audio data stream remains free from errors and due to the way PT's playback tone decoder works, only responding to signal transitions, the polarity of the ½ cycle of 600 Hz tone recorded or the full cycle of the 1200 Hz tone is unimportant in the tape playback & data recovery process.

Playback Processing Circuitry:

The processing of the recovered or played back tape tones has to reverse the process described above for recording. In other words the tape tones must be converted such that a 1200Hz tone becomes a logic 1 and a 600Hz tone a logic 0, so as to regenerate the serial data for the UART's input pin. It is a much more complex process to do this well than creating the recorded tones.

Also there are synchronization issues related to the timing of the tape signals, versus the timing of the computer's system clock. Another requirement is that the original clock frequency (responsible for the recording) has to be regenerated in a stable manner so as to track changes in tape speeds either with the same tape deck or between different tape decks, to make sure that the UART's read clock stays in step with the recovered data. In addition there is a large variation in amplitude of the played back signal level presented to the SOL-20. And there are issues of noise immunity and the ability to successfully decode poorer quality recordings. The Sol-20 circuitry has methods to help deal with all of these potential problems:

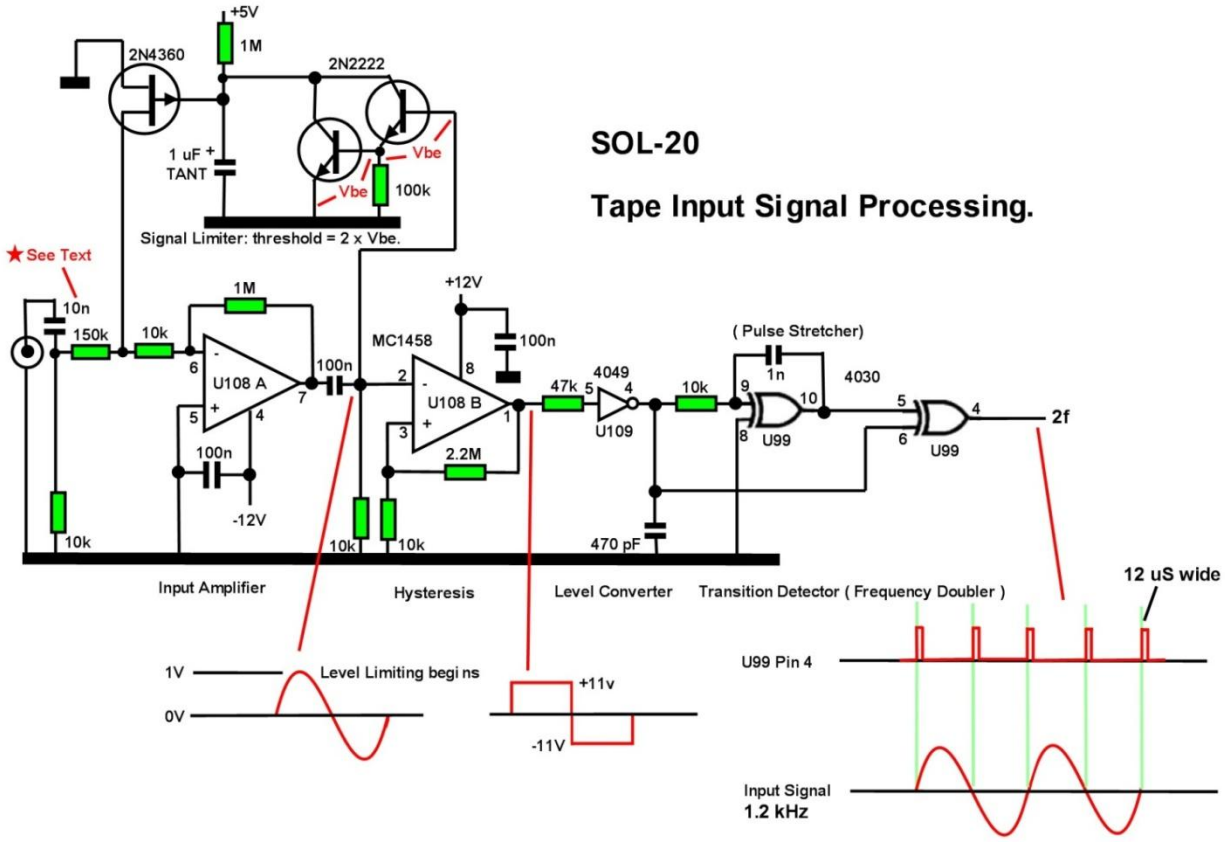


Fig. 3.

The circuitry, Figure 3 above, shows how the played back tape signal is initially processed. The incoming audio signals passes via a voltage divider (which includes the source-drain resistance of a 2N4360 p channel depletion mode Fet to ground). The negative input of the OP amp U108-A acts as a virtual ground.

The analog signal directly from the tape player must be converted into a digital or pulse train format that corresponds to the frequency of the played back tones and have all amplitude variation eliminated. As noted above, the original recorded signals were not perfect square waves but rounded off a little with filtering. (When testing the Sol's tape input circuits, a lab audio Sine Wave Generator is perfectly adequate).

While it would appear that an OP amp configured as U108-A would provide an approximate inverting voltage gain of about 1 Meg/ 160k or about 6.25 (in the absence of any effect from the limiter circuit) it does not. Even with the Fet's gate at +5V, the Fet is not completely cut off and some of the input signal is divided down. There is also some loss of signal level due to the low frequency roll off provided by the 10nF input coupling capacitor. (There is also a phase shift due to this low value, see below).

Therefore, prior to any significant limiting action provided by the FET circuit, with about 700mV peak applied at the input connector, the output voltage (pin 7 of U108 A) is only just reaching about 1V peak.

If the input level is increased above about 700 mV peak, then the peak voltage at pin 7 drives the combination of the two base-emitter junctions of the two 2N2222's into conduction, discharging the 1uF capacitor and lowering the Fet's gate voltage. This decreases the Fet's source to drain resistance and shunts more of the input signal to ground. The base emitter junctions of the 2N2222's, for *small signals*, start to conduct around a voltage of 0.5 to 0.55V, not the usual 0.65 to 0.7V drop seen for higher base currents. This is why the amplitude limiting effect starts at around the 1V peak signal level at the output of U108-A.

If the input *peak voltage* rises above about 700mV, the peak amplitude seen at pin 7 levels off to about 1V. There is a remark in the SOL Systems Manual that the voltage is levelled to 2 volts peak, but that is a misprint and it probably meant to say 2V "peak to peak".

Below 700mV peak at the input jack, the levelling circuit is inactive as there is not enough peak voltage at pin 7 to get the 2N2222 transistors into conduction. This circuit is better thought of as a "signal amplitude leveller or limiter" with an input threshold voltage of about 700mV peak rather than an "AGC", but that might be semantics.

Since the circuit involving U108-A and the 2N2222's and the Fet, in the 1200 Baud mode at least, is to "amplify and level" a 600 Hz and a 1200 Hz tone, it is a little

surprising that the 10nF input coupling capacitor, coupling into an impedance just below about 10k, perhaps around 9k, is such a low value. The 3dB cut-off frequency is 1/(2.pi.R.C) or about 1770 Hz, so there is moderate loss of signal level because of the 10nF value being low, especially for a 600 Hz tone. But obviously, it still works, though it may have been better if it was a 47nF or 100nF and not a 10nF. However, one ameliorating factor is the actual tones are more rectangular than a sine wave, and the decoder circuits are only interested in the transitions of the signal, not the low frequency response.

Therefore, to test if the input signal amplifier and signal leveller is working, apply a 1200 Hz test tone to the input connector J7, from a sine wave generator and monitor the voltage on pin 7 of the OP amp U108. Below 700mV peak level (at the input connector J7) pin 7 will follow the amplitude changes. However above about 700mV peak, the voltage on pin 7 will level off to close to 1V peak and ignore amplitude increases at the input after that threshold has been crossed.

Moving along, the signal then passes to the comparator U108-B which squares it up into a +/- 11V amplitude square wave. The hysteresis (positive feedback) around this comparator sharpens up the rise and fall times to give a very square looking wave and improves the noise immunity.

All of the *amplitude variations* of the input signal are now eliminated. One way to quickly convert the +/- 11V signal to a 5V logic level is to pass it to a cmos logic inverter gate (U109) via a large value resistor (47k). The input protection diodes on the cmos gate prevent the gate input voltage from going below zero volts or above the +5v supply rail. (This inexpensive “trick” which avoids a level converter IC, is sometimes also used to convert RS-232 logic levels into 5V logic levels in an RS-232 receiver circuit).

The signal then passes to the two XOR gates U99, configured as a switching transition detector. An XOR gate produces no output when both of its inputs are at the same logic level. However, if one input is delayed a little with respect to the other, at the time of a signal transition, the XOR gate will produce a pulse during that delayed time. Since the signal “transitions” twice per cycle, then the frequency of the recovered signal in now doubled. (This does not matter as it is divided down again later with a flip flop).The pulse width measured at U99 pin 4, is around 10 to 12uS

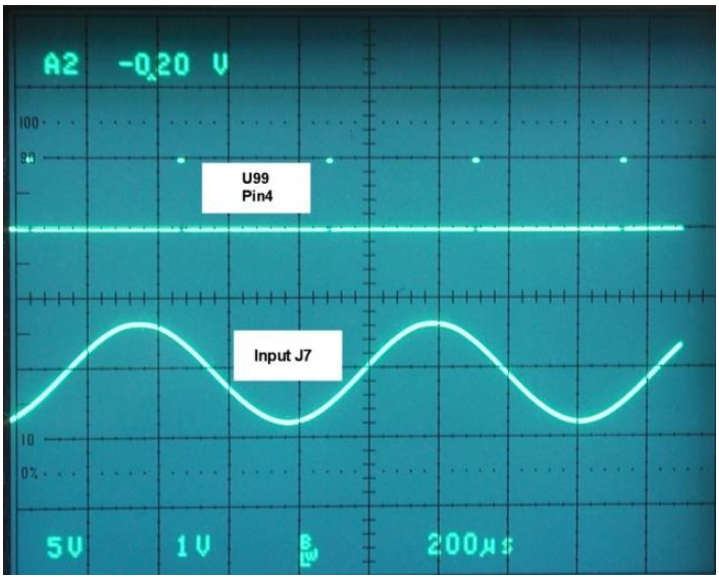


Fig. 4-A

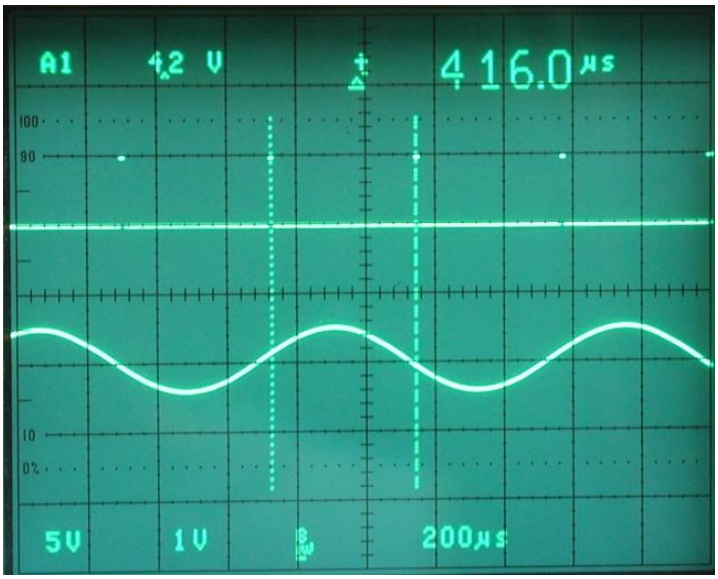


Fig. 4-B

Figures 4 A & B above are an oscilloscope recording of the input voltage at J7 and the output voltage at U99 pin 4.

Notice something interesting in figure 4A, the pulses from U99 pin 4 are not occurring near the zero crossings, where one might expect, with respect of the timing of the input waveform on J7. This is due to the phase shift that occurs due to the 10nF input coupling capacitor. It is of no consequence in terms of decoding the tape data. Figure 4B shows the input waveform measured on the opposite side of the 10n input coupling capacitor, the amplitude is lower and most of the phase shift is absent as expected.

Now that the recovered tape signal is in a form of digital pulses it is a matter of processing it to 1) discriminate between two frequencies and 2) allow for speed variations of the played back tape which affect the exact frequency of the pulses and 3) regenerate the original serial data clock rate, to enable drift free receive clocking of the UART.

For this discussion the frequency rates of the 1200 Baud mode will be discussed for the most part. Also it pays to remember that the frequencies fed into PT's tone decoder circuit (from the output of U99 pin 4) are *frequency doubled* with respect to the 1200 and 600 Hz tones on the actual tape itself. PT's circuit is shown in figure 5 below and looks deceptively simple.

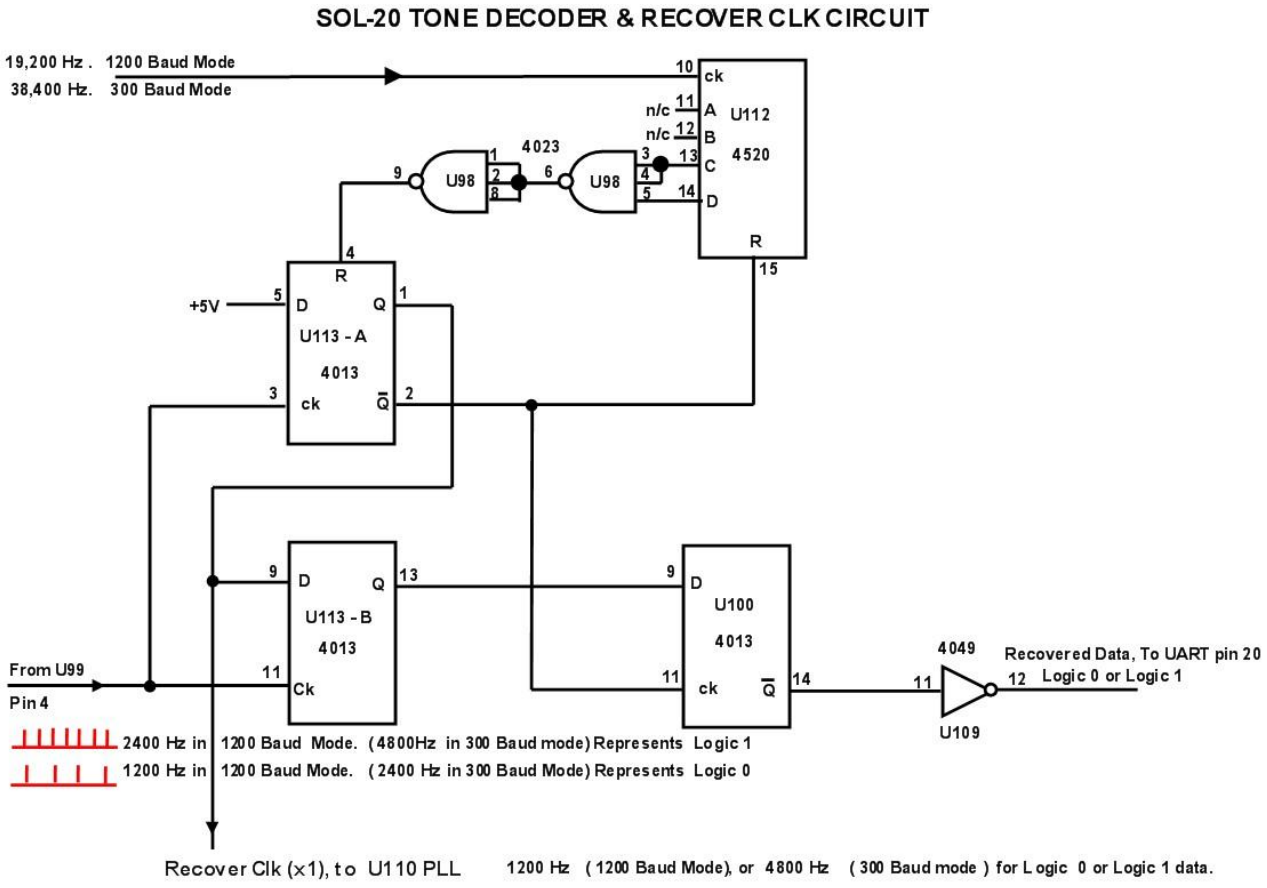


Fig. 5

Firstly, the original 1200 Hz clock rate, a signal called Recover Clock (x1), which is synchronised to the tape tone transitions must be regenerated (and later stabilized) to provide a read clock to the UART. This is the job of U113 – A and U112. The trick being to regenerate the 1200Hz rate, regardless of whether the actual tone recovered from the tape is 1200Hz or 600Hz. The timing diagram below, figure 6A, shows how this is done, *using two continuous tones as examples*:

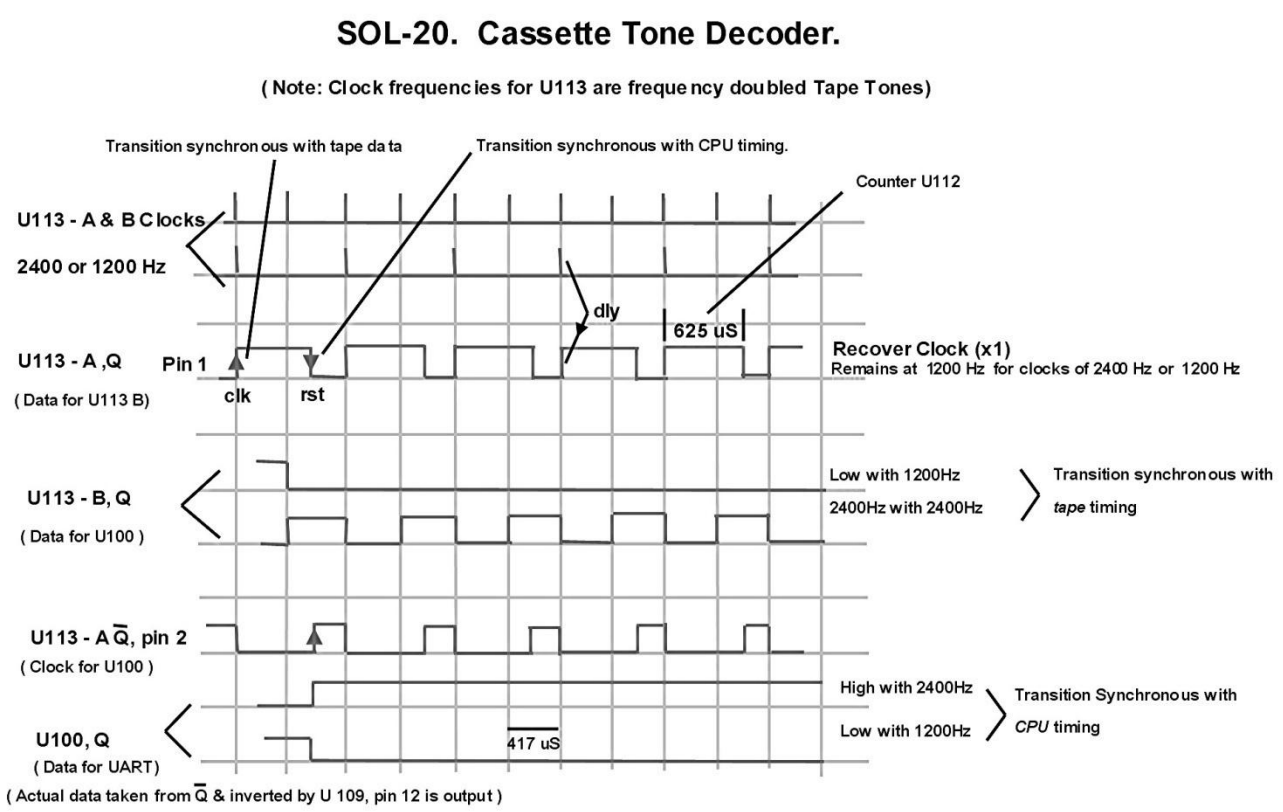


Fig. 6A.

The frequency doubled playback tape tones clock U113, both sections A & B. A counter (U112) is set up and clocked by the 19200 Hz reference pulse from the Baud rate generator (recall that this signal is locked by a PLL to the divided down computer master clock). The 625 uS delay created by U 112 allows U113-A to be reset only after a second clock pulse occurs (if the frequency is 2400 Hz). So U113-A only responds to every second clock pulse if the pulses are 2400 Hz, or every clock pulse, if they are 1200 Hz.

This means (in 1200 Baud mode) that the output of U113-A (pin 1) the Recover Clk (x1) as PT labelled it, *is always 1200Hz*, regardless whether the recovered tone from the tape is 1200 Hz or 600Hz. So this makes the Recover Clk (x1) equivalent to the clock pulse of the recording system (that clocks U101 A & B) and it represents a regenerated version of it.

In addition, the leading edge (positive going) of the recover clk(1) pulse is synchronous with the tape tone transitions. However, the falling edge, is created by the counter reset loop in conjunction with U113-A. At the point that this timer/counter reaches 12, the

reset begins synchronously with the clock pulse of U112. This clock pulse has a different timing origin. It is derived from the 19200Hz Baud rate generator (which is frequency synchronised to the computer's system clock. Therefore, looking on the scope, it is normal for the Recover Clk (x1) waveform to have a moderate phase jitter. So do not be alarmed if that is seen on a scope recording, it is not a malfunction. The amount of jitter seen depends on the exact frequency of the incoming tone.

The tone decoder/discriminator works by applying the recover clock signal at the data input of flip flop U113-B. The timing diagram of figure 5 shows the Q output of U113-B for the two cases for the two clock signals corresponding to the two recovered tones. Because there is a propagation delay from the time when U113-A is clocked and its Q and /Q output change state (shown as "dly" in the diagram), then at the time Q113-B is clocked the Recover Clk(x1) is still low at that time. So a low is clocked to the Q output of U113-B. On the other hand, if the clocking signal is 2400Hz, a High is clocked to U113-B's Q output, because the Recover Clk (x1) pulse it high at that time.

U113-B's Q output acts as the data for U100 and the clock pulse is /Recover Clk (x) or the inverted version of the recover clock. As a result a low is clocked to U100's /Q and generates a High on U109 pin 12 if the tape tone is 1200Hz and a Low if it is 600Hz. (the reverse of the recording process).

On account of this, the tone decoder system is very easy to test. A sine wave signal generator is applied to the tape input connector J7 with an amplitude of 500mV peak or more and the frequency varied from 600Hz to 1200Hz. U109 pin12 should be logic 1 (high) with a 1200 Hz tone and low with a 600Hz tone.

U100 is clocked by the inverted Recover Clock signal, this timing edge is frequency locked to the system clock as it is derived from the 19200 Hz signal from the Baud rate generator. Therefore the timing of the logic high and logic low transitions that the UART receives, on its input pin, are frequency locked to the computer's Baud rate generator in this design.

Also of note: Although figure 6 shows how the tone decoder works to identify two different tones, it does not readily indicate how quickly the circuit is able to do this. We know it must be able to detect a half cycle of the 600 Hz tone and change its output nearly immediately to generate a logic 0. This requires a different timing diagram to show what happens when the tone changes from 1200 Hz to 600 Hz and back to 1200 Hz again, corresponding to the serial data bits it represents being 1 0 11 as an example. (This diagram also explains why PT decided to frequency double the tones from the tape in their decoder circuit, without this it would not have been possible to process a ½ cycle of the 600 Hz tone). The timing is demonstrated in figure 6B:

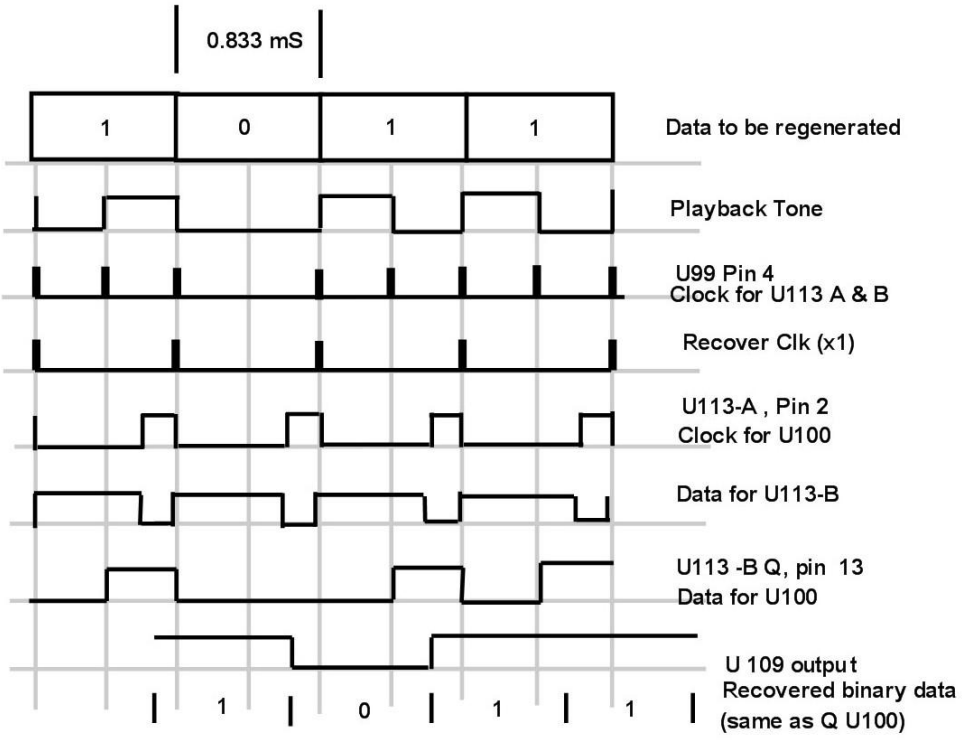


Fig. 6B

U113-A produces clock data for U113-B. U113-A's outputs change state *after* the rising edge of the clock pulse due to the propagation delay. So if it appears on the diagram that a clock pulse clocking U113-B is coincident with the rising edge of the pulse on its data input (derived from from U113-A) then U113-B does not clock a logic 1 to its Q output at that time, because the data is not actually high at that point.

Clocking the UART:

In the ***transmit*** mode the UART is clocked (Byte Write Clock on its TC pin 40) by 19200 Hz in the 1200 Baud mode and by 4800 Hz in the 300 Baud mode. These signals being derived from the computer's Baud rate generator.

In the ***receive*** mode the UART is clocked by Recover Clock (x16) at 19200 Hz in the 1200 Baud mode and 4800 Hz in the 300 Baud mode.

The Recover Clock (x16) signal is generated by the output of a 4046 PLL IC, which is locked to a x16 multiple of the Recover Clock (x1) signal described above. This is so that the UART's receive clock rate, tracks the speed of the tape and it doesn't creep out of step.

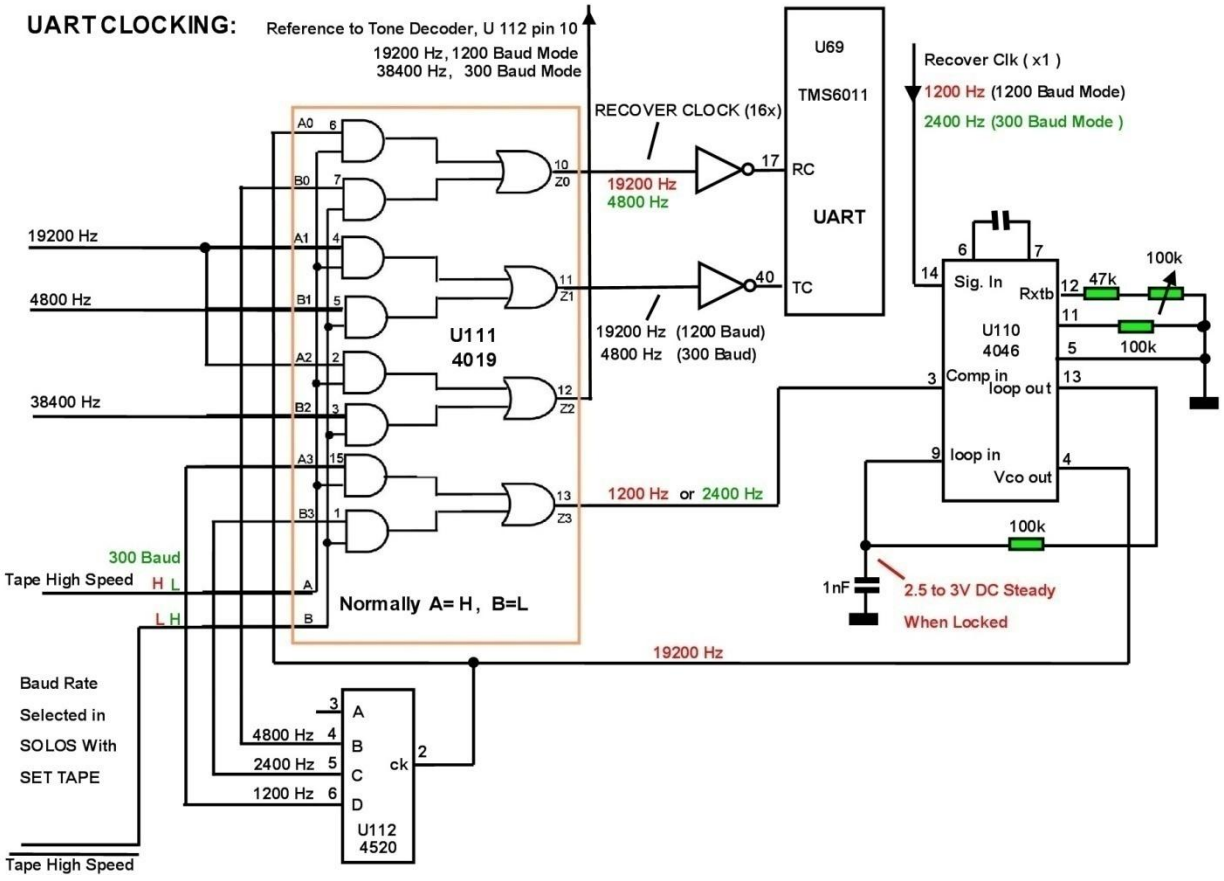


Fig. 7.

Also the PLL effectively acts as a temporal filter and eliminates most of the phase jitter of the Recover Clock (x1) signal, the leading edge is synchronous with the transition of

the actual tone signals recorded on the tape. Figure 7 below shows the arrangement. The values in red are for the 1200 Baud mode, those in green show the 300 Baud mode and relate to frequencies ultimately sourced from the tape. The values in black have a computer origin.

This Statement appears in PT's hardware manual page VIII-34:

For *high speed*, the divide by four output of U112 (pin 4) is selected as RECOVER CLOCK. For *low speed*, the VCO output of U110 is selected for RECOVER CLOCK. This clock serves as the read clock for the UART, U69.

This is an error and the words "*high speed*" and "*low speed*" should be swapped.

Possibilities for Recovering Damaged Tapes:

Since PT's tape decoder system relies on detecting signal transitions and it also regenerates what would have been the original clock rate/signal (for both 300 Baud & 1200 Baud tapes), with a stable PLL there is an opportunity.

If the output of the PLL was subject to a phase adjustment circuit and also associated with a timing window or gate operating at 1200 Hz, the playback tape signal transitions could be gated through that. Then any large noise pulses or tape damage might be largely ignored, because the circuit would then only respond to a signal transition, in a zone, where there would be expected to be one in the 600 and 1200 Hz pulse sequence. I have not tried this idea yet, but it would be good to retrieve any damaged recordings from old tapes, if possible.

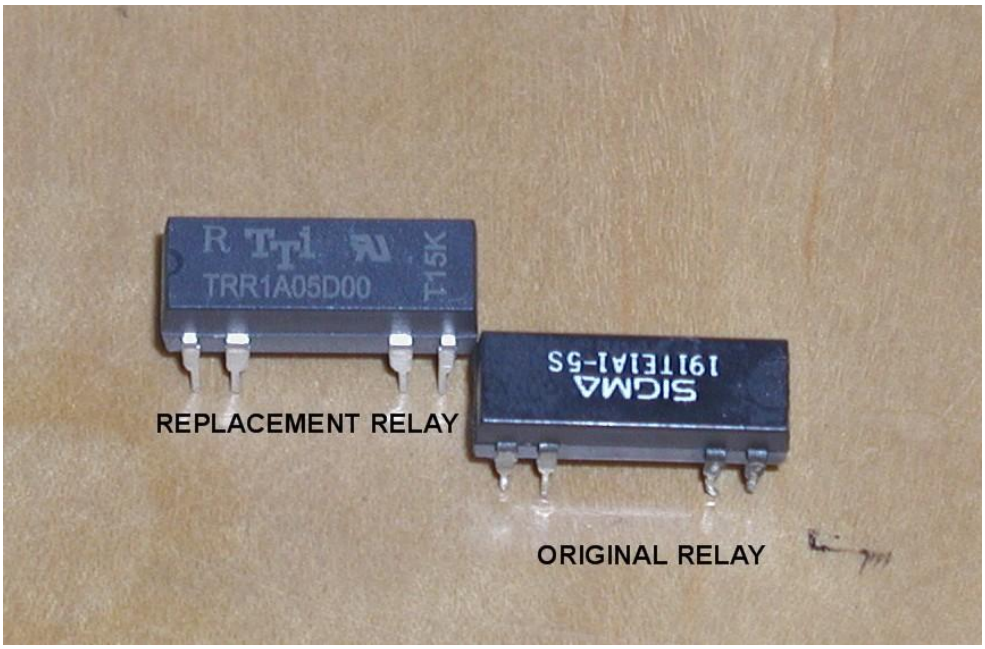
Sol-20 Tape Recorder Remote Control Relays:

Small 5V DIL relays (with a 500R coil) are used on the Sol-20 main board to control the stop/start activity of the tape decks used.

The remote connection is used to start the tape deck prior to the beginning of a recording or playback and also to stop the deck after the end of the file which is being transferred. This is done by connecting the relay contacts (via the 2.5mm remote Jacks) to the remote input connector of the cassette player.

These relays have a contact current rating of 1A, which seems a fairly high rating for their physical size.

The photo below shows the original relay used in the Sol-20:



PT made a modification to the Sol-20, by adding 6.8R resistors in series with the relay's contacts, the explanation being to prevent the relay contacts becoming welded together. My Sol-20 did not have these resistors fitted.

I had initially tried my Sol-20 with a Panasonic RQ-2765 slimline cassette recorder. All seemed well initially, until as predicted by PT, the relay contacts welded themselves

together. This required replacement of the relay. I fitted machine pin IC sockets, with three cental pins on each side pressed out of the socket, so I could easily replace the relays in future if the same problem occurred without removing the Sol-20 main board from the case again.

Looking at the design of the motor switching circuit in the Panasonic tape recorder, there were a number of things that were not ideal. Also PT's solution by adding the resistor was not ideal either.

In the Panasonic recorder, the remote jack was connected directly in series with the negative connection of the motor, which is a mechanical governor style of motor, typical of small cassette recorders.

I checked the motor current; around 80mA to 100mA on playback and about 350mA when stalled, which the motor draws initially when attempting to start the motion of the cassette and the mechanism from a stopped state. With a 6.8R resistor in series with the motor, the voltage drop across the resistor is about 2.4V in the stalled state and sometimes this slows the start of the tape especially if the cassette is a little sticky. So the series resistor idea, that PT chose to protect the relay contacts from over-current, is not an ideal solution.

But why would the series resistor be needed if the maximum motor current is only 350mA and the relay is rated at 1A, how could that cause relay contact failure? The answer was obvious on inspecting the circuit in the cassette recorder:

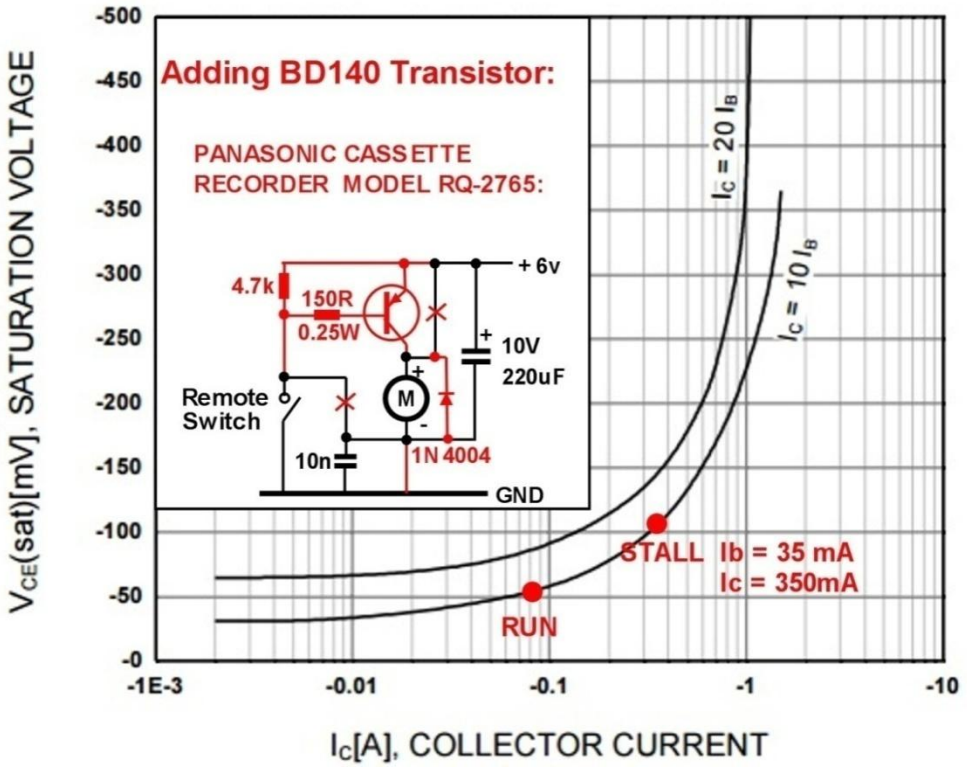
There is a 220uF 10V capacitor in parallel with the motor. A capacitor like this would normally have an ESR of around 0.3 Ohms.

In the tape recorder, the designers had also added a 0.47R resistor in series with the power supply & battery supply to the unit. Taking this resistance into account and the resistance of the wiring and running the recorder from four C sized Alkaline cells, the brief peak initial current (due to the 220uF capacitor's initial charging current) via the remote jack could exceed five Amps when the motor starts. This explained why the relay contacts in the Sol-20 relay welded themselves together.

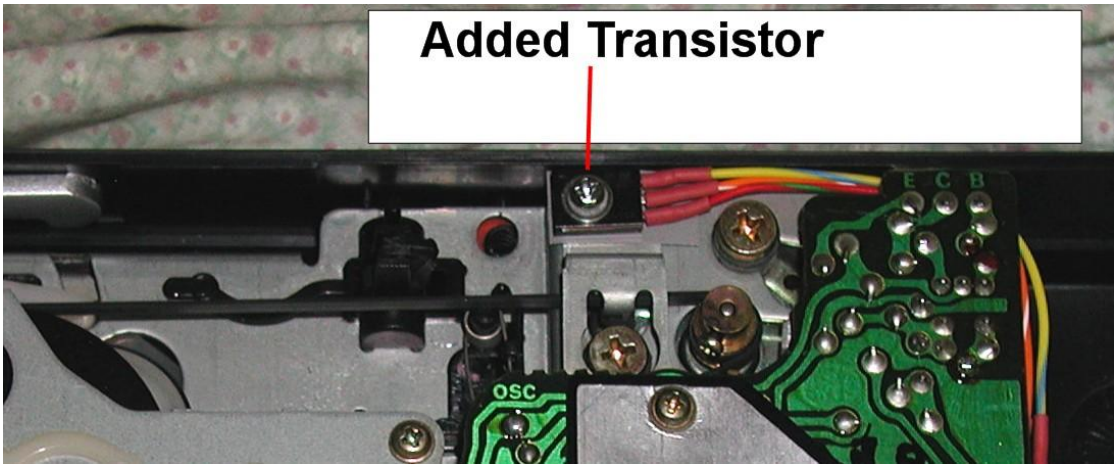
This also probably explains why PT chose the 6.8R series resistor value because it limits the peak relay contact current to around 1Amp or less, when the cassette recorder runs from a 6V supply, which they typically do. I concluded from the above information that the cassette recorder would be better modified by adding a transistor to switch the motor and take the load off the small relay contacts in the Sol.

A simple modification to the cassette recorder was made, using a BD140 transistor that could be screwed down to an existing screw. A diode was also added to absorb any

voltage transient when the motor switches off and two resistors are required. The diagram below shows the original (in Black) and modified wiring (Red):



As the graph above shows it is quite easy to get the BD140 transistor into heavy saturation for collector currents of 350mA or below with 35mA of base current. This means that even for the motor in the stalled condition, the voltage drop across the transistor is close to only 100mV. This is far superior to the series 6.8R resistor idea that drops 2.4V.



Of note, since the damage done to the small relay contacts is largely due to the charging current of the 220uF electrolytic capacitor when the contacts close (and not the motor current) one solution could have been to have placed a 6.8R resistor in series with the 220uF capacitor, so that excessive charging current did not flow via the relay contacts in the Sol. However, this may have worked out not so well because the idea of the 220uF capacitor is to help filter out interference from the motor and the effect would be reduced by adding series resistance to the capacitor. Another option might have been to go for a smaller filter capacitor for the motor, such as 1uF, the peak current would then be for a shorter duration, reducing the chances of the relay contacts becoming welded together, but it is still less than ideal.

I’m not sure of the exact design of the motor switching arrangements, via the remote jack, in other small tape recorders of this type, but likely they will be similar. In any event it would pay to check how the motor is switched on & off in the particular cassette recorder to be sure that the miniature relay contacts in the Sol were up to the task, or at a bare minimum, have the 6.8R resistors installed in series with them as PT recommended.

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