THE PAL FREEZE FRAME MACHINE.

Dr. H. Holden. July 2017.

Background:

The first time I saw a video image frozen at the touch of a button was on a Dr. Who episode in the late 1960's when I was about 9 or 10 years old. It was as though the Time Lord had frozen time. He pushed a button and the image he was watching on a black and white video monitor froze. I was very impressed.

I had considered that this freeze facility would be great to have incorporated into a home TV set and I wanted one. Perhaps it is partly true that all things come to those who wait.

With a freeze frame machine the image of an object of interest could be frozen for inspection before it was gone forever. Often interesting images from live TV were not often repeated in those days and home video recorders didn't exist yet. I had no idea at that young age how a video signal freeze frame could be accomplished or even where to start to design such a machine. Though, at that point, I had built a few simple radios and tinkered around with some valve TV circuitry and received numerous electric shocks.

Another application of a freeze frame machine has been used by Hollywood in the movies & TV. The scenario was sometimes seen in vintage TV shows, such as Mission Impossible and featured a freeze frame device. Typically there is a closed circuit TV camera looking at some top security area. The secret agent or similar attaches a circuit board to the camera's video output feed, it captures & freezes the image and outputs it down the camera cable. So the security guard watching the monitor in the control room sees what looks like a normal situation, while in reality all sorts of antics are going on.

One could argue that the two original "electronic video special effects" were freeze frame and a negative picture. Later the number of video effects skyrocketed with split screen and "picture in picture". Movement and rotation of images in video memory soon started to dominate the video effects in TV advertisements. Colorization of grey scales was another early video effect. Once computer manipulation of video data in computer memory space occurred, it led to fantastic innovations in the video gaming industry and also animated movies such as those made by Pixar and the latest Planet of the Apes trilogy where the graphics are incredibly lifelike. The revolution continues with virtual reality headsets. CT & MRI scanners were also realised with video data manipulations.

Over the years of course, it became a very easy task to freeze a video image, if the video material was recorded at least, because nearly all types of video machine or DVD player had a pause button. Once digital TV arrived the live image could also be simultaneously recorded and live-paused.

In addition, computer “frame grabber” cards became available from the 1980’s onwards so as to capture video still images. Many early versions of these cards simply captured one field of the video signal. Later frame grabber cards became more sophisticated, capturing a frame (two fields) and then able to handle multi standard colour signals and then entire video recordings and movies. However these require the computer and supporting software to operate and in many cases the captured image is only for a computer screen display or computer data manipulation.

Solid state video recorders have also become popular in the security industry and the recorded video images can be stepped through frame by frame.

Despite the advances in technology, the problem still remained in my mind of how to build a simple electronic machine to capture or freeze a frame of video and make it self contained and independent from a computer. Initially I just wanted to do it for a monochrome video signal for vintage television applications, but of course once the project was started, ambition set in, it had to work for colour as well.

This article describes the design of a 2, 4 or 8 field PAL video store or Freeze Frame Machine, based on the field store IC, the Averlogic AL422B.

Requirements of a Frame Video Store for PAL Colour and Monochrome Images:

The minimum requirement to store a basic video image is to capture one field. However, single field capture results in an inferior quality image compared to storing and displaying two fields, or a frame of a video image. This is because significant data is missing and as a result serrated edges appear along diagonal lines in the image, though interpolation can help this problem. Despite this, there is one advantage; the captured image is largely free from motion artefacts because it is captured over a 20 milli-second time frame.

It is best for a quality monochrome still image, to capture *two* fields over 40mS. However, there is more opportunity for motion artefacts in the image, but a better quality image, especially if there is little motion in the image that is captured.

In the PAL system there are 8 unique colour fields, so 8 fields must be stored for a perfect PAL colour still frame. It can actually be done with a 4 field store with a small initial burst & colour phase error, upsetting the video monitor’s PAL decoder momentarily at the start of vertical scan.

(In the case of capturing NTSC colour, the burst phase is unique at the start of 4 fields. This means there are two even and two odd fields which have a different burst phase. So to reproduce a perfect colour NTSC still image, it requires the readout of 4

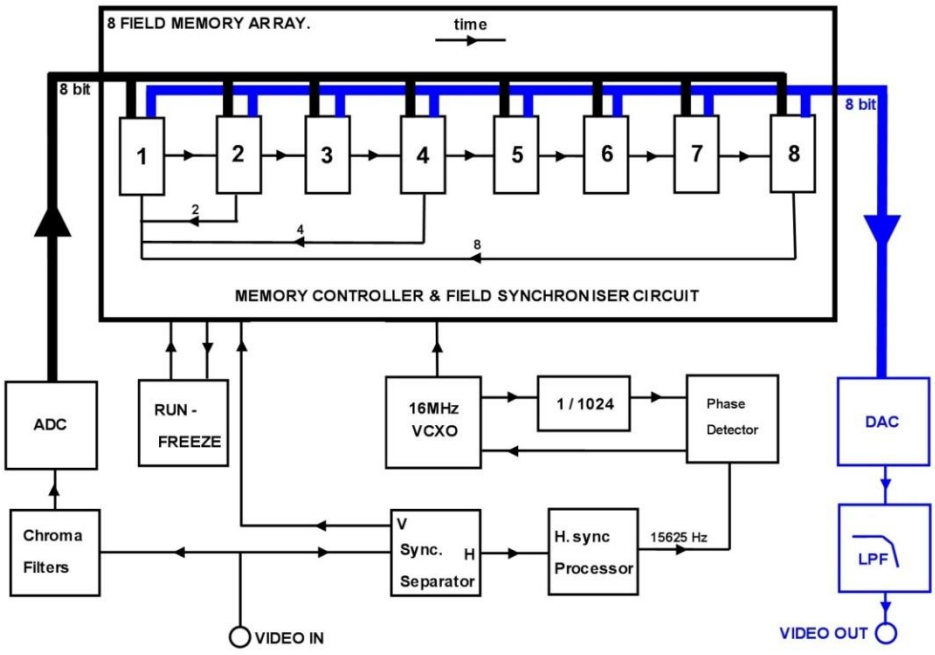
consecutive fields. To make this unit work with NTSC all that is required is the crystal is changed from 16.000000 MHz to 16.111888 MHz and the 1/320000 divider chain changed to a 1/268800 divider).

The machine described in this article has been made to be able to optionally store 2, 4 or 8 fields. Also built into the circuit are Chroma filters to filter off unwanted colour sub-carrier signals when just a monochrome image is desired and when the source video signal might be colour. These chroma signals can cause unwanted patterning effects along the edges of rapidly changing luminance signals.

Many devices which digitize analog video, such as Time-Base Correctors and Standards Converters strip the sync off the video signal because after the processing a new stable or altered sync is inserted. Also, often, the colour signals are processed separately from the Luminance signal and they are recombined later if a composite video signal is required.

To increase the simplicity for the freeze frame machine described here, the entire incoming composite colour video signal is digitized to retain both the picture luminance information, sync pulses and colour signals. Despite the complexity of a composite colour video signal, it is still an analog signal which can only possess one amplitude value at any one moment in time. It does require a stable line (horizontal rate) locked master crystal oscillator (pixel clock) to digitize the video to memory and to read it out again in a stable fashion so as to avoid phase errors which degrade the colour sub-carrier. Much less stability is required for just a monochrome image frame store.

The very basic block diagram below shows the arrangement of the freeze frame machine:



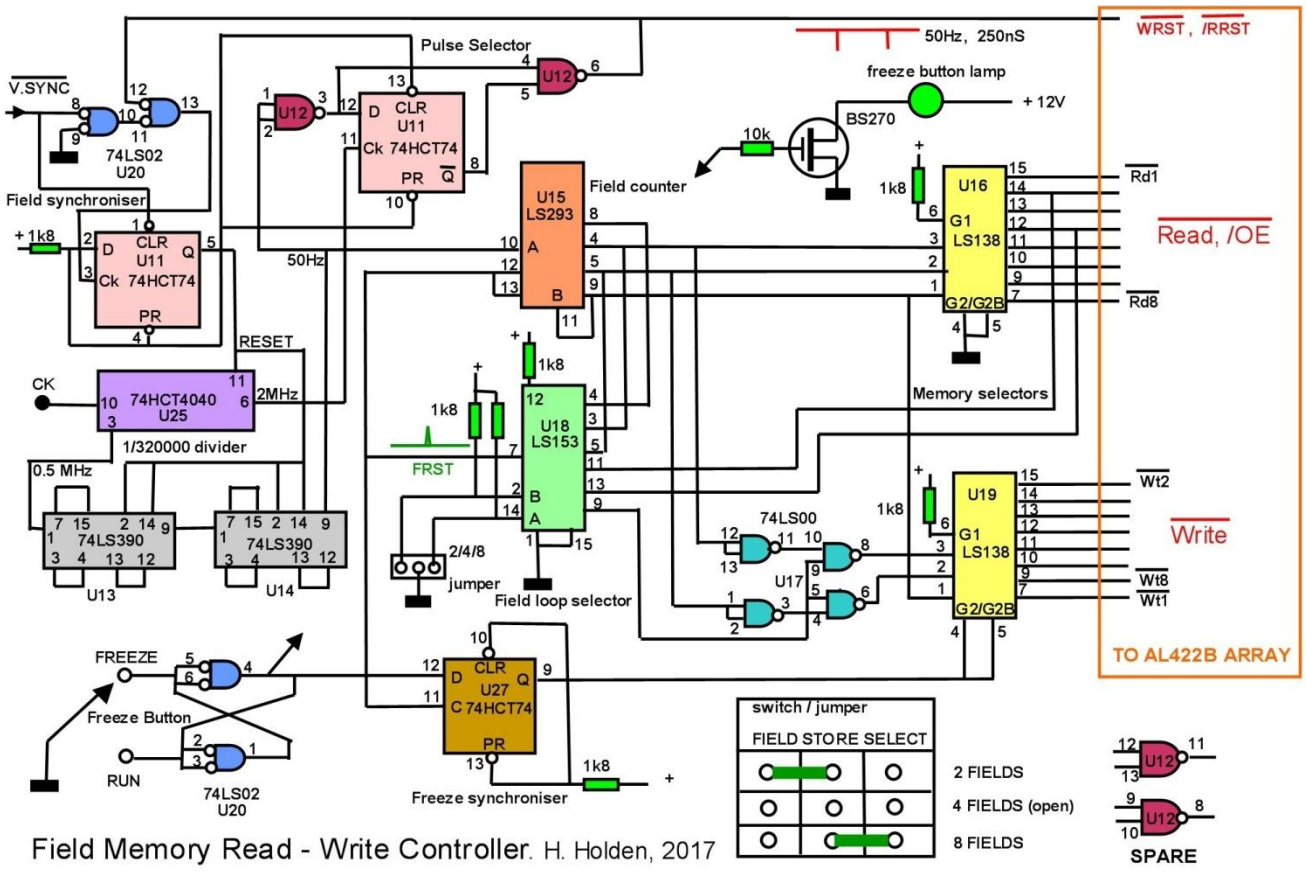
Generally, when digitizing any analog signal it is important that the sample rate (pixel clock frequency in this case) is at least twice the maximum analog signal frequency. In the design presented here, the sample rate chosen was 16MHz, well over twice the upper expected high frequency component in the colour video signal. Higher sample rates generate more data and use more memory space, however there is the advantage that the output from the digital to analog converter is easier to filter and in this case it was achieved with an off the shelf 5MHz low pass filter module.

As can be seen from the block diagram above there is a horizontal (line) locked 16 MHz master oscillator or pixel clock. This phase locked loop is achieved with the 1024 divider and a phase detector.

Inside the memory controller, the pixel clock is also divided by 320000 to generate a stable 20mS pulse to the field memory controller circuits for resetting and switching between the AL422B's for each field. Initially I had attempted to use the vertical sync (from the sync separator) for this task, but this was a mistake because the vertical sync signal carries too much phase jitter to be successful for a colour version of the freeze frame machine. Burst phase and colour errors occurred at the top of the picture just after the field switching point.

Of note and not always shown in the schematics below, every IC has, on its power supply and earth connections, a 100nF monolithic ceramic bypass capacitor. The power supply & earth connections for much of the digital logic are omitted for clarity.

The memory controller (diagram below) is arranged to be writing a field to one memory IC, while the IC in the chain behind is being read. So the writes are in advance of the reads by one field. The controller arranges 2, 4 or 8 fields to be read and written while looping back to the first memory IC after the last field write. This is selected by a front panel switch or pcb jumper.



Field Memory Read - Write Controller. H. Holden, 2017

The 74LS153 is used as a data selector to control the reset cycle of the 74LS293 binary counter for the 2,4 and 8 field selection. Two 74LS138's are used to decode the counter outputs to select the appropriate AL422B memory writes and reads. When the particular AL422B is read its output is simultaneously enabled with /OE and is disabled at other times as all the IC's share the same output data bus.

To have the writes in advance of the reads, the write '138 outputs (physical connections) are rotated forward one step in the chain of 8 memory IC's.

To ensure the correct IC is selected to be written next after the end of the 2 or 4 field selection, 2 bits from the write '138 are encoded to alter the three bit count data feeding the write '138. This is done wiring a 74LS00 (U17) as a data selector. The end of the 8 field selection automatically returns the correct write sequence to the first AL422B in the chain.

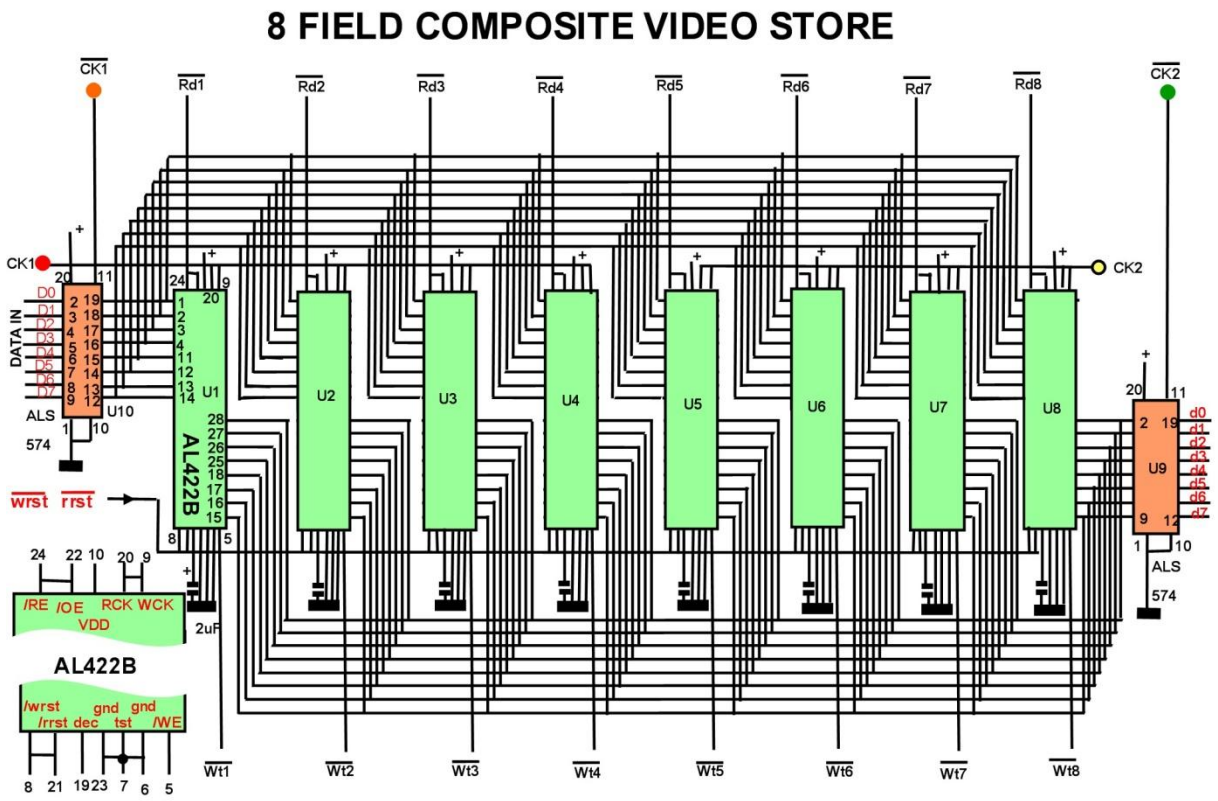
One job of the read-write controller is also to ensure that when freeze is selected it happens exactly at the end of the write time for the last IC in the 2, 4 or 8 selected chain. This is achieved with the freeze synchroniser flip flop U27.

Another important circuit within the memory controller is the field synchroniser. Without the synchronizer, the switching point between fields can occur anywhere in the field and it is sometimes visible as a tiny winking dot of less than a microsecond disturbance somewhere in one scan line. To solve this it required that the switching point between fields be synchronised with vertical sync, in a manner where it was just done once each time an incoming sync signal was presented and would only re-deploy after a sync dropout. U20 and U11 create a detector which has zero output when the memory reset pulse and vertical sync pulses are coincident. If they are not, U11 pin 3 is clocked and the 320000 divider is reset and is held reset by U11 and not released until U11 pin 1 is cleared by the /vertical sync. This ensures the 320000 counter starts counting on the leading edge of vertical sync, but remains free of the phase jitter of the actual vertical sync itself.

U12 and the other half of U11 form a pulse selector circuit to create stable 250nS reset pulses for the AL422B memory IC's. This is a classic pulse selector circuit commonly used in TTL video games to select a single clock pulse or other pulse related to the clock from the a lower frequency timing edge.

When the controller is in the run mode, the video effectively just appears to pass through the unit from the video input to the video output. But it is delayed by one field.

The schematic below shows the memory array:

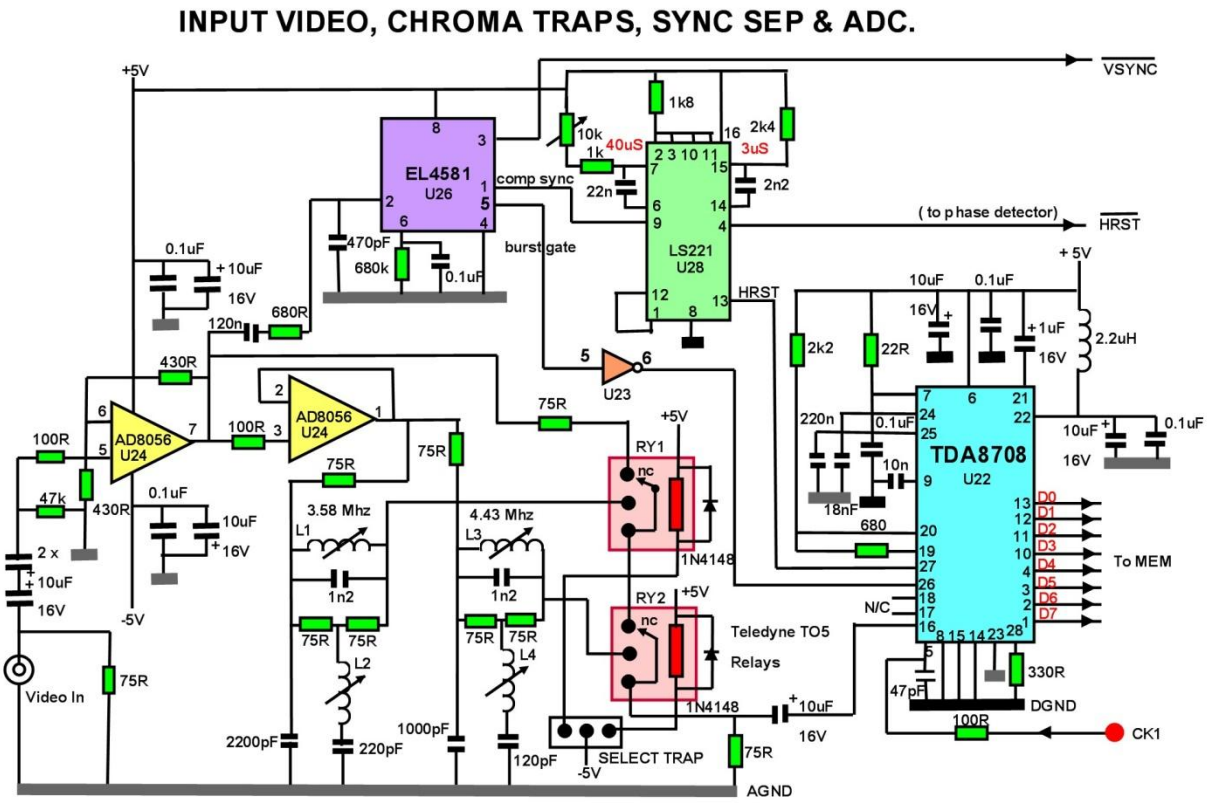


Of note, the AL422B is very helpful for this application because it contains its own internal address counters which are automatically incremented with the clock pulse. In this case the read and write counters are *both* reset by the one 250nS reset pulse generated by the memory controller circuit.

(The read & write control of the AL422B is independent so that they can have different timing, making this IC also very useful for standards converters or time-base correctors as well for anyone considering designing one).

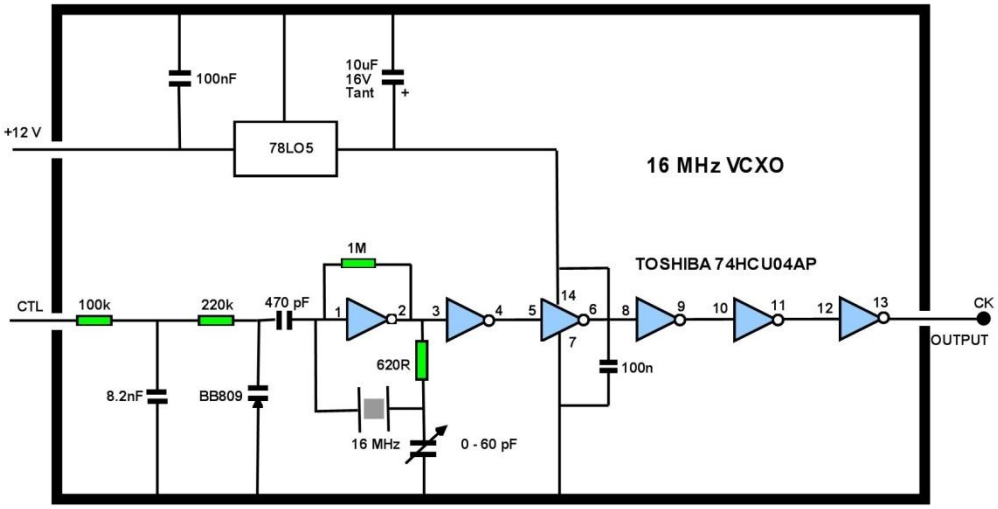
The AL422B is a 392,216 (384k) x 8 bit Fifo. Using a 16MHz clock and 20mS time per field, the number of 8 bit memory locations used per field is 320,000 so there is still some room to spare when storing a whole field in each IC at this high pixel clock rate.

The 74ALS574's that buffer the memory I/O are clocked by an anti-phase clock signal compared to the memory IC's. This is so that on the output side the data is stable before it is clocked out to the DAC and on the input side it is clocked from the TDA8708 ADC IC into the memory, only after it is definitely stable. The circuit below shows the input signal processing:



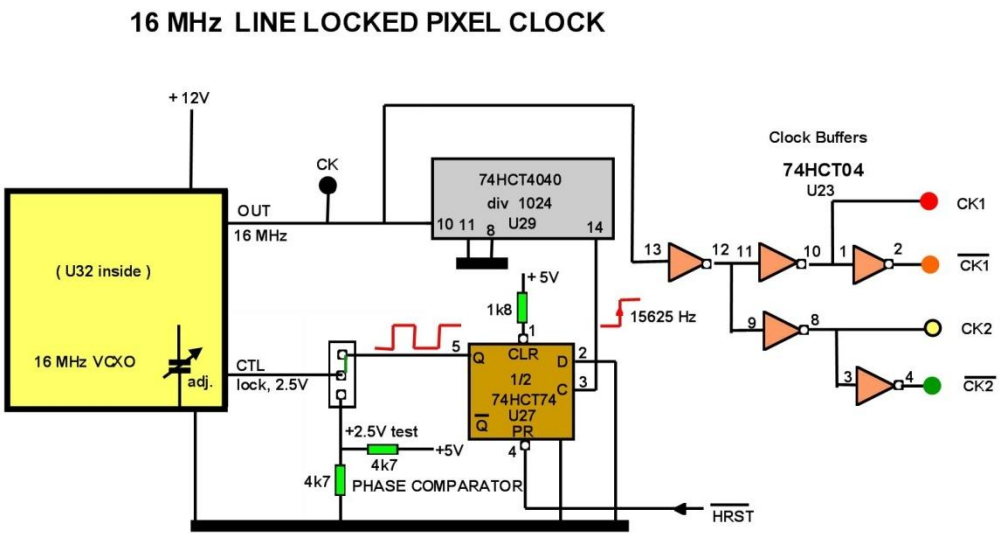
The input video processing is fairly standard. There two independently selectable chroma filter options, though the one used for PAL is generally the 4.43MHz. The application of the dual monostable U28 is to remove the vertical sync pulses and equalising pulses from the composite sync signal. This way there is no change in the error voltage control of the line (H) locked 16MHz VCXO oscillator during the vertical sync period.

The circuit below shows the master oscillator or pixel clock. This VCXO was built into a fully shielded enclosure with its own separate voltage regulator:



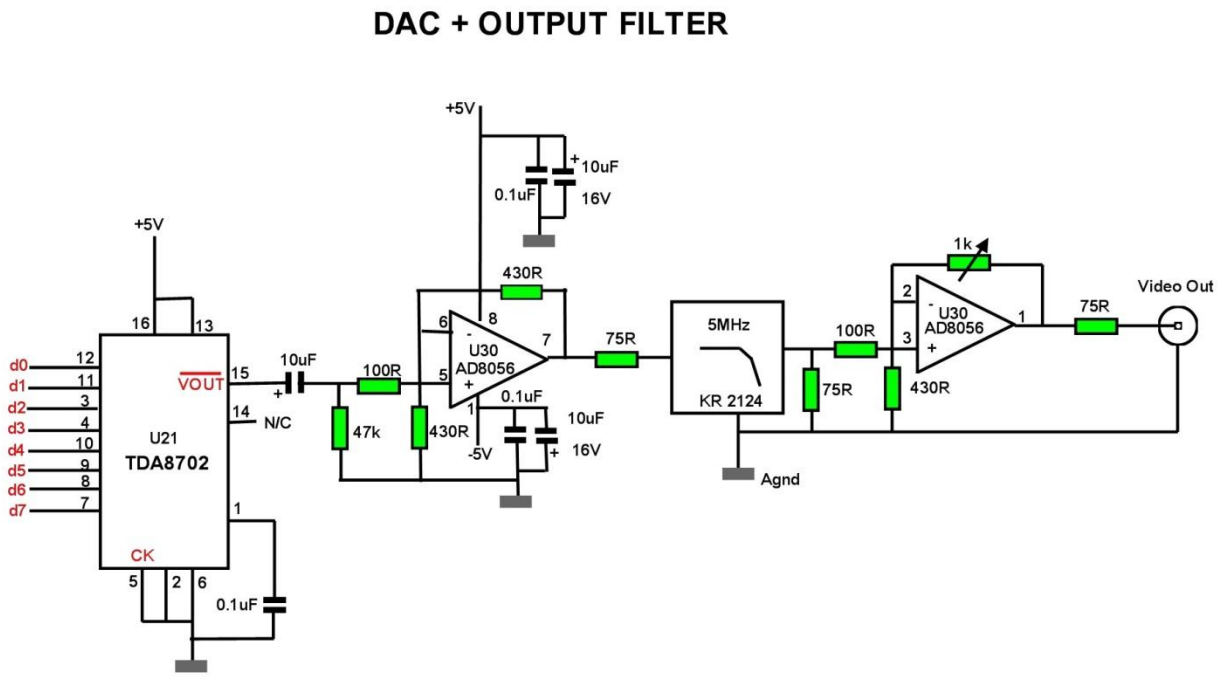
For a crystal oscillator based on cmos gates it is helpful if the un-buffered type is used. The 1M feedback resistor biases the buffer into Class A to form an effective inverting amplifier, hence the 74HC”U”04.

This oscillator is combined with a phase detector to form a PLL. Also additional buffers are used.



The phase detector U27 is created from a 74HCT74 which was chosen because its output stage has a full rail to rail swing, unlike a 74LS74. The 16MHz clock is divided by 1024 (by U29) to 15625 Hz and this clocks the Q output of U27 low. The /HRST pulse from U28 sets Q high. As a result when the 1024 divided VCXO and the horizontal sync of the incoming video signal are locked in a 180 degree phase relationship the Q output of U27 is a square wave. This is square wave is integrated to control the vari-cap diode in the VCXO to result in stable phase lock.

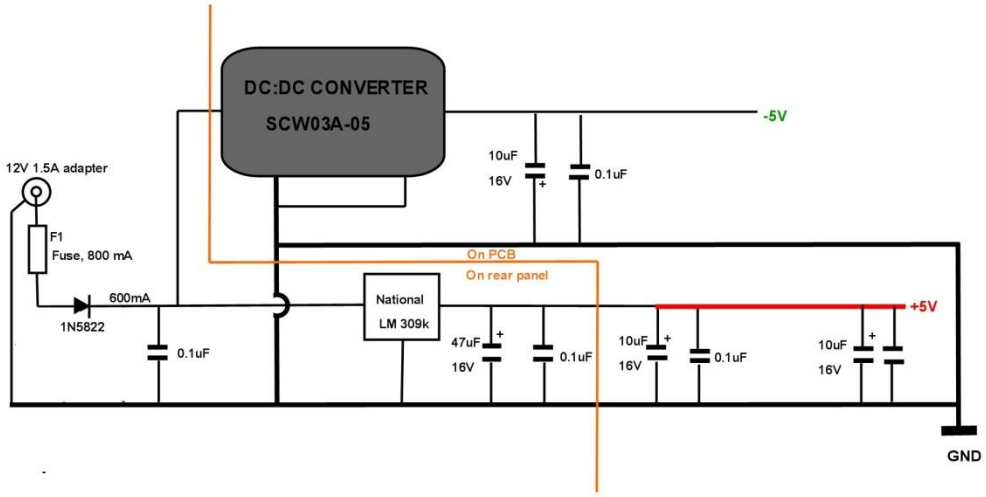
On the output side of the unit there are very few parts:



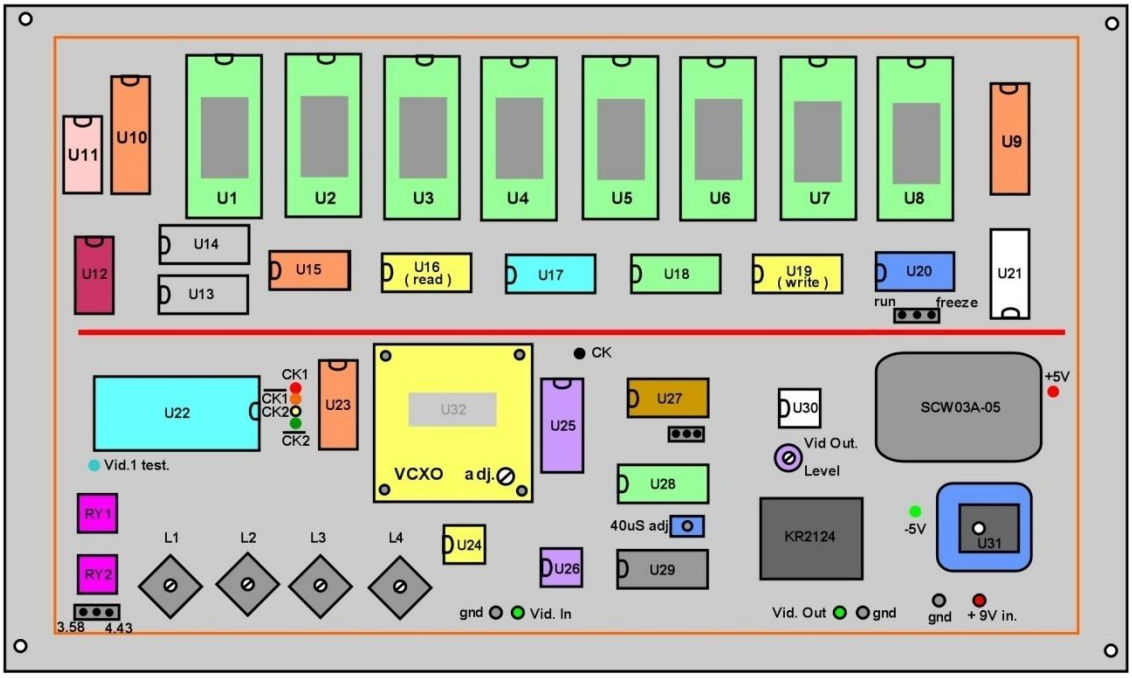
As noted before, one advantage of the higher clock frequency is the ease which the digital output can be filtered. The KR Electronics KR2124 5 MHz LPF module is used for this application.

The power supply is very simple as shown below. To generate the -5V negative supply rail a DC:DC converter was used. Initially I started with a 7805 regulator on the circuit board (U31), but due to the overall 600mA current consumption and the heat dissipated in this, I moved the regulator to the rear panel and used instead a 1970’s vintage gold plated National Semiconductor LM309k. This was placed in a high quality Augat panel socket for mounting. These sockets also provide handy soldering lugs for components near the regulator.

POWER SUPPLY.



The diagram below shows the location of the major parts on the circuit board. The board is plated through hole spot board that is 232mm x 137mm in size. The bottom surface is wired with point to point contacts, with tinned copper wire, following patterns similar to a PCB tracks. Elsewhere it is wired with miniature Teflon coated wire (like that used for wire wrapping) however all points were soldered. For a good result each wire was prepared by removing the insulation near its end first, tinning the wire with solder and then fitting the wire between connection points. This way, all the connections are very neat and reliable.

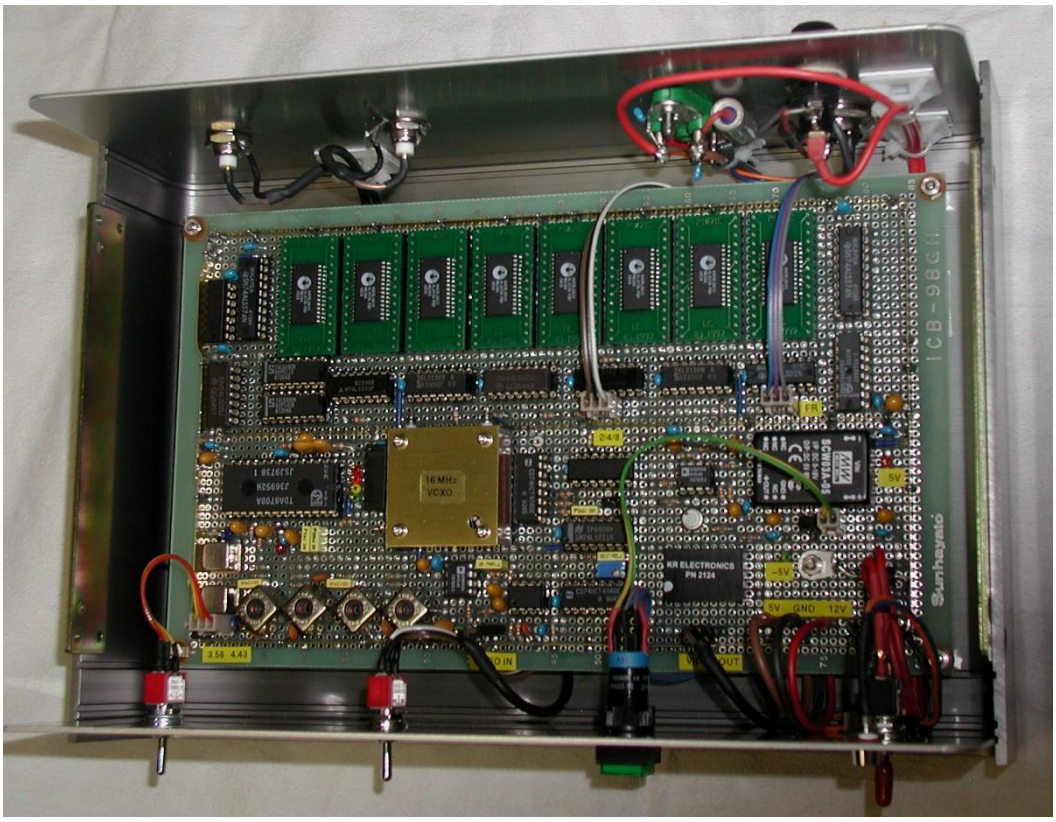


Fitting the circuit board to a Takashi extruded aluminium case:

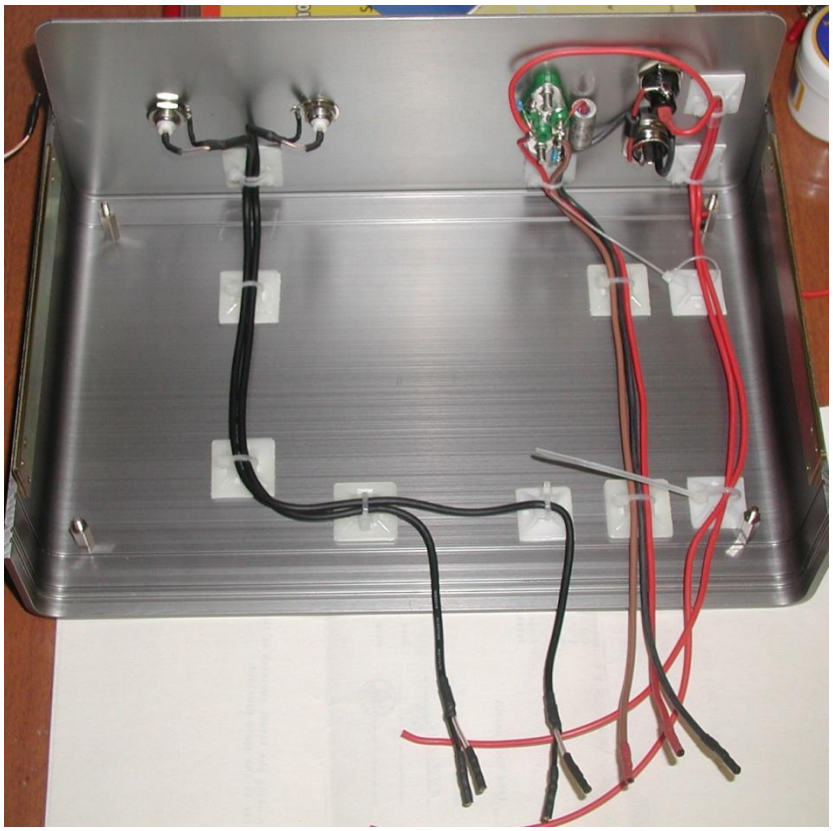
The photo below shows an oblique view of the inside of the unit to help avoid camera flash reflections.

All of the front panel switches are attached with plugs to the circuit board. The circuit board connections otherwise are single 0.9mm gold plated single plug & socket fittings (these are Jaycar Eelectronics parts).

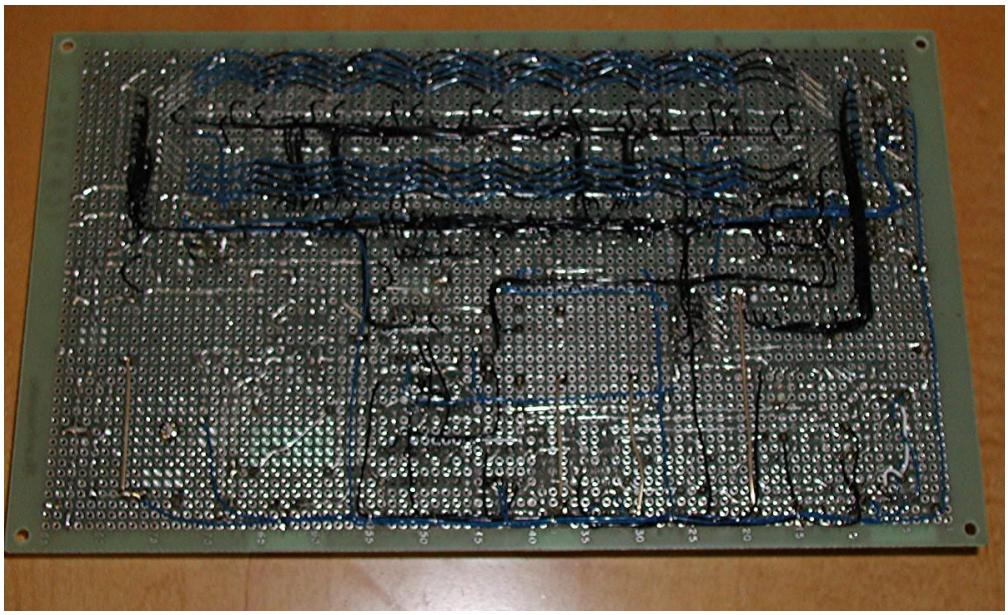
A somewhat ceremonious freeze switch was used which is a push button switch with an internal lamp for illumination. To facilitate this, a BS270 Mosfet was added to switch the lamp.



The photo below shows the unit under construction. The screws that mount the 4 nickel plated brass post to the case also serve to secure the case's rubber feet, the feet have an internal metal bush. No electrolytic capacitors were used in the construction of this unit.



Finally, the photo below shows the wiring on the underside of the hand wired board:



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