

INCREASING THE UTILITY OF THE IBM 5153 COLOR MONITOR TO AUTO-DETECT AND DISPLAY A 9.5" DIAGONAL 16 COLOR 21.85kHz EGA IMAGE.

Dr. H. Holden, April 2016.

Introduction:

If the IBM 5153 monitor is driven by an EGA card, set to run in CGA mode, for the most part all is well. However some software packages (such as Draw Partner) or other types of software flip the card into EGA mode or an EGA screen. At that time the image on the 5153 scrambles and loses both H and V lock. This is because the EGA has an inverted vertical sync pulse and a horizontal scan rate of 21.85k Hz versus the 15.75 kHz scan rate for the 5153 color monitor.

The IBM 5154 monitor solves this problem, being a dual standard monitor that fully supports the EGA scan rate and EGA color system as well as CGA. However the 5154 is rarer and more expensive than a 5153. Also, not enough attention was paid to thermal management and ventilation of the cabinet in the 5154 and a number of the components get thermally stressed and overheat the phenolic pcb's, especially in the region of the video output stages and the vertical deflection output IC in the 5154.

The 5153 is constructed from high quality components. The pcb's in the 5153 were made by Tatung and use many quality made Japanese components. Also, the 5153's internal metalwork is better quality than the 5154; it has a better thickness and electroplating than the metalwork in the 5154. The 5153 had additional ventilation slots in the rear of the cabinet and the heat generating resistors were kept well clear of the pcb surfaces. The physical build of the 5153 was better in my view than the 5154 even though the 5154 had much more utility value.

The designers of the 5154 were very smart in separating the horizontal scan output stage from the stage generating the CRT's EHT (normally in monitors this stage is common). This is because a change in the horizontal scan mode has significant effects on the EHT and ideally the EHT is stable. Also it was quite a feat to build a dual standard monitor like a 5154 and the idea of this at the time was relatively new, so I think the 5154 for those reasons gets credit there. The 5154 also had very good reviews in its day compared to other non IBM EGA monitors which shows that its performance was leading edge.

The idea of this project is to have a workable/usable EGA image auto detected and displayed on the excellent and well built 5153 monitor. This modification is primarily

mediated by an additional pcb that is added inside a standard IBM5153 monitor on existing mounting holes. Negligible modifications are made to the monitor itself, only 5 minor easily reversible changes.

The added “control pcb” auto detects the presence of the EGA signal and alters the parameters in both the vertical and horizontal scanning systems to increase the Horizontal scan rate to 21.85 kHz and reduce the horizontal flyback time to suit EGA image reproduction. This gives 15 accurate colors (see below). With a very small additional “color 6 fix” pcb, with one IC, Color 6 is corrected to give an accurate 16 color EGA image.

The article is divided into six sections:

SECTION 1: Image resolution issues.

SECTION 2: The “control pcb” schematic and circuit functionality.

SECTION 3: Correcting Color 6 with a “color 6 fix” pcb.

SECTION 4: Results and screen photos of 16 color EGA images on the 5153:

SECTION 5: Scanning & flyback technical issues and Captain Nero’s Red Matter.

SECTION 6: How to correctly set the 5153 monitor’s own H.Hold and H.Phase controls.

SECTION 1.

Image resolution issues:

Ultimately, despite the on-off digital nature of the R,G & B digital drive signals presented to the inputs of the R,G & B gun amplifiers, the CRT display monitor is an analog device. Even when the amplifiers are driven with a square waveform, as the frequencies increase at the upper limit, the resulting drive waveform to the CRT's guns becomes sinusoidal as the amplifiers are unable to produce the higher frequency odd order Fourier harmonics which would be required to regenerate a square waveform.

It is interesting to look at the factors which determine the resolution of the screen image.

Vertical resolution:

This is set by the number of viewable scanning lines on the CRT face which relates to the focused beam geometry. There is really no issue for a "multi-standard" monitor for the CRT's used in 5153 or 5154 monitors. These CRT's could, if required, easily produce a 525 or 625 line image for NTSC or PAL video. Therefore a 200 or 350 line image is little of a challenge. Even with a reduced sized (9.5" diagonal) EGA image, the viewed scanning lines just "touch" so little is lost in vertical resolution.

Horizontal resolution:

As suggested above, the amplifiers driving the CRT's electron gun have a limited bandwidth as all amplifiers do. Could this be a limiting factor in attempting to get the 5153 to display an EGA image in a high scan rate mode ?

The bandwidth limit of the gun amplifiers in the 5153 could possibly limit the resolution in a high scan rate mode, so this question was investigated first.

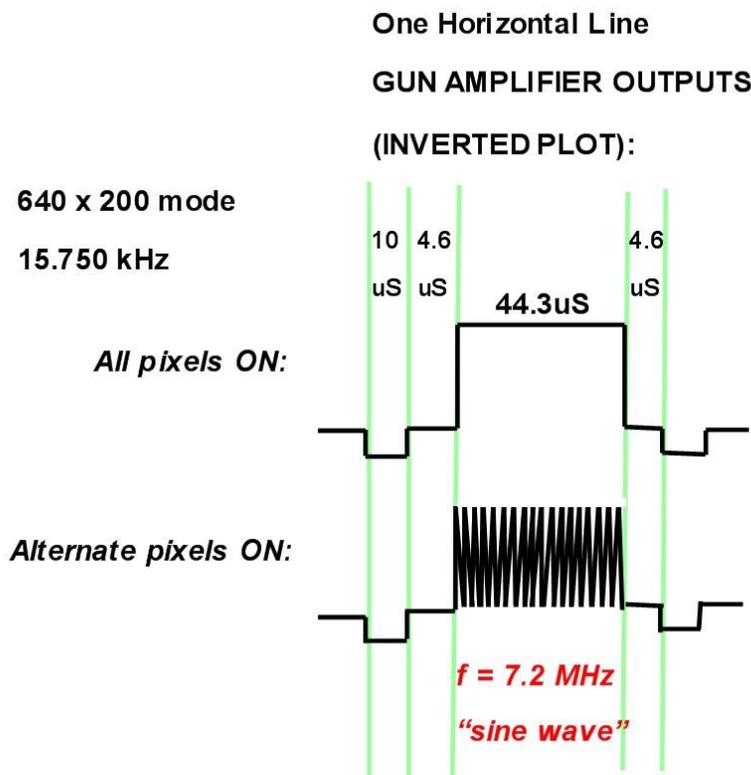
Generally bandwidth values are stated for the frequencies (usually the upper value) where the signal amplitude has dropped down 3dB (about 70%) below the mid frequency range gain value. Looking at the frequencies involved:

Firstly looking at a 640 x 200 graphics screen (screen 8 in Basic) which is a 15.750 kHz line rate screen. In this screen if ALL the pixels are switched on along one horizontal (H) scanning line by pixel setting 0 – 639 to ON, there is actually no high frequency alternating signal at all along a horizontal line. The GUN drive is held on for the whole length of the scanning line. The H scan period is $1/15.750$ kHz or 63.5 μ S. The length of this plotted line in time is about 44.3 μ S, the horizontal blanking is around 10 μ S and there is about 4.6 μ S of unused scan time on each side. (So in this mode the whole available screen horizontal scan time is not used).

The diagram below shows this. The upper frequency that must be supported by the GUN amplifiers occurs when *ALTERNATE* pixels are switched on so that the pixel sequence is ON-OFF-ON-OFF etc across a horizontal line. The “acid test” for resolution therefore occurs when alternate pixels are illuminated.

(The 10us period on the diagram below is the horizontal retrace time).

As the diagram and measurements show this alternate pixel pattern has a frequency of 7.2 MHz in the 15.750 kHz mode because 320(the number of on-off cycles in one horizontal line) divided by 44.3uS is 7.2 MHz:



Examining this drive waveform at the gun amplifier outputs (Using a very capable Tek 2465B 400MHz bandwidth scope) the waveform appears sinusoidal, not rectangular and the sinusoidal part has an amplitude of 19V.

Repeating the same tests for an EGA screen 9 in basic:

In this screen (on the modified 5153 monitor) the horizontal retrace time is shortened to around 6uS and the scan period being 1/21.85 kHz or 45.7uS. This leaves a horizontal

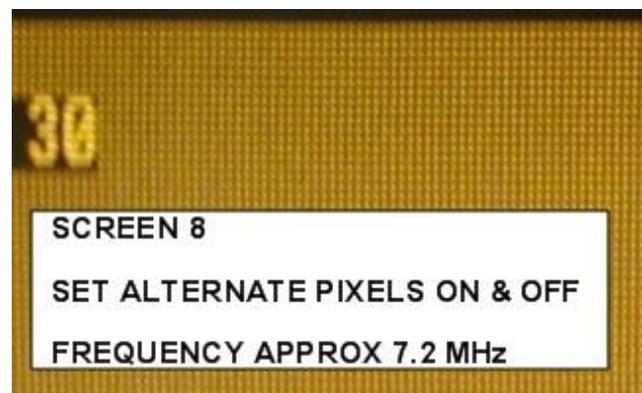
display time of around 39.7 μ S. In this screen when pixels are plotted all the available active scan time is used and a plotted line starts right at the beginning of scan time. The frequency of alternate plotted pixels is close to 320/39.7 μ s or 8MHz. Checking with the scope this is correct and the measured amplitude of this signal is 18.0V, only slightly reduced from the 19V value of the 7.2MHz signal of the 15.750 kHz mode.

In other words in high scan rate mode, the video amplifier frequency response is only about 5 to 6% down in level for the EGA screen compared to the CGA screen.

The above findings indicated that the video bandwidth of the gun amplifiers in the 5153 (despite any published bandwidth specifications) is perfectly satisfactory for displaying the high scan rate EGA screen graphics even though they were not intended for this purpose and perhaps not quite as good as those in the 5154 but very close.

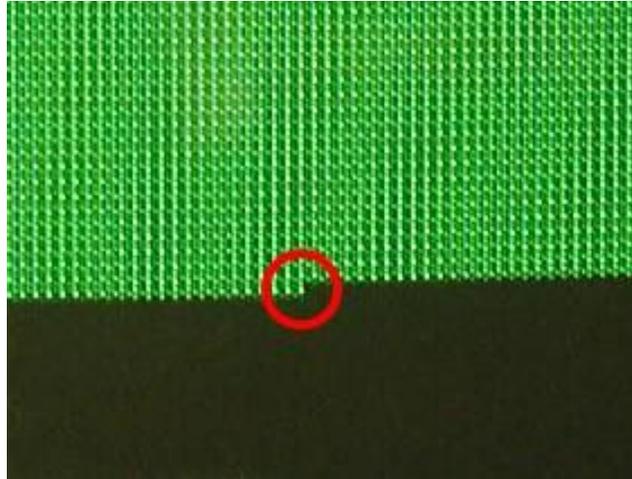
What about the color CRT itself, focussed beam and shadow mask considerations?

Firstly, for a comparison, the photo below shows a screen 8 image of the amber monochrome CRT in a 5155 computer with alternate pixels lit. The small focussed beam diameter with respect to the CRT screen size, is such that it is actually possible to see the alternate lit pixels, although there is light scatter into the dark pixel areas making them look narrower than the lit areas:



Unfortunately, Color CRT's such as those in the 5153 or 5154 are not generally capable of exactly this sort of resolution. While the phosphor pitch in the CRT from a 5153 or 5154 monitor is small enough to support such a display resolution, the limitations imposed by the CRT's shadow mask and focussed beam diameter are such that a single pixel is not as well defined and the phosphor dots (from phosphor trios of the same color) in the local area are partially illuminated.

For example if the same ON-OFF-ON etc pixel pattern for a 640 x 200 image is displayed (in one color, green for this example) on the 5153 in the usual 15.750kHz mode (which is said to support 640 pixels) the following result is obtained:



Due to the width of the electron beam and the shadow mask geometry, single green phosphor elements are not the only ones lit, there is a spread around the phosphor trio into the adjacent six green phosphors, making the illuminated pixel less well defined than in a monochrome CRT. Also with tri-color pixel illumination, convergence errors cause a larger spread around what would be the pixel center.

Therefore the limiting factor in horizontal resolution, be it the 15.75 kHz mode, or the 21.85 kHz mode, is the design of the CRT itself. Fortunately in the 5153 the color CRT was rated for 640 picture elements on a horizontal line, just like the CRT in the 5154 and the resolution is acceptable for both CRT's regardless of the operating mode being EGA or CGA.

In this article for brevity I will call the low scan rate (15.75kHz) mode "CGA mode" and the high scan rate (21.85kHz) mode, "EGA mode"

SECTION 2.

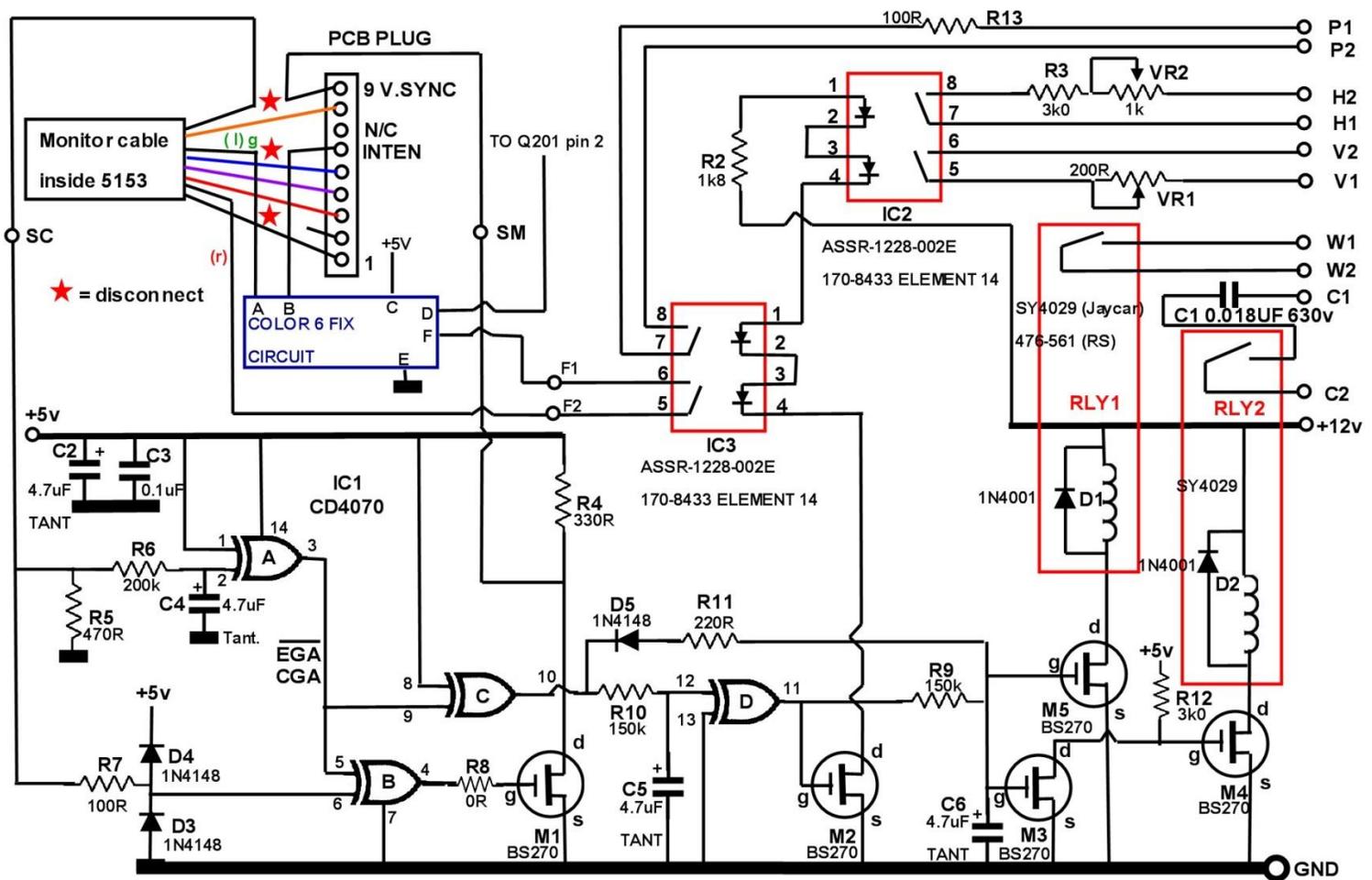
Control PCB schematic and circuit functionality:

Firstly, the concept was to have a control pcb that drops into the 5153 monitor, mounts in a convenient location (using existing holes) and has an array of connections that simply reach out to various points of the 5153's circuit.

The intention was to not significantly or irreversibly modify the 5153 monitor. Some of the connections on the control pcb are terminals that project from two relays on the pcb.

There are some very minor changes required to the 5153 as will be shown. None of these changes have any significant influence on the usual function of the 5153 monitor in CGA mode, but assist in the functions when it changes into EGA mode.

The schematic of the added pcb is shown below:



AUTO-DETECT 16 COLOR EGA DISPLAY FOR IBM 5153. H. Holden. April 2016.

Circuit Description:

The connections of the cable are broken into near the cable plug by cutting the wire about 1 inch from the plug and joining wires to the cut ends insulated with heat shrink sleeving.

The cable wire to pin 9 is the vertical sync input from the cable labelled SC. This sync signal is filtered for its DC level by R6 and C4 and passes to pin 2 of gate A.

In CGA mode (a positive going sync) the waveform, on the average, has a low DC level, so the output of gate A pin 3 is high. The sync also passes to gate B and since pin 5 is high gate B inverts the sync and it is again inverted by mosfet M1 and therefore returns normally to the monitor pcb connector pin 9, connection SM.

When the sync polarity inverts (in EGA mode) pin 3 of gate A falls low, so gate B is no longer inverting, and M1 inverts the sync to the correct polarity again for pin 9 of the connector on connection SM. So regardless of the mode, the 5153 monitor only sees (receives) a positive going vertical sync on connection SM.

Gate C inverts the low (present in EGA mode) to a high. This charges the delay network R10 and C5 until the threshold of gate D is reached. Gate D's output then goes high switching on mosfet M2 which turns on the two Photomos relays IC2 and IC3. These solid state relays result in the horizontal scan rate being increased to 21.85 kHz, and the horizontal phase and vertical height being adjusted, as well as an input from the r LSB picture signal being coupled to the "color 6 fix" pcb.

Also after another delay accomplished by R9 and C6 RLY1 is switched on, shorting out the width control inductor to gain the maximum possible width in EGA mode. Also RLY2 turns off disconnecting the 0.018uF tuning capacitor connected across C419 on the monitor's pcb. This leaves in circuit, in C419's location, a 0.001uF 2kV rated capacitor that was inserted in place of C419. This reduces the flyback time in the horizontal output stage in the EGA mode (see section 5).

Most EGA computer video cards attempt to place the r (LSB) signal on pin 2 which is grounded at the monitor's pcb plug in the 5153. (For the IBM card there is a jumper can be removed which isolates this connection). In this case we need access to pin 2 (for a color 6 fix circuit) so the wire from the cable to pin 2 is cut and joined to a long wire to pass to the added control pcb on the opposite side of the monitor.

The intensity connection to the monitor cable is also broken into in a similar manner to pass to the nearby small "color 6 fix" board.

Overall, in summary, detecting EGA results in the following changes:

- The H scan rate is increased to 21.85kHz and potentiometer adjustable (VR2).
- The flyback tuning capacitance is reduced to allow the shorter flyback time.
- The width coil is shorted out to partially compensate the large width reduction.
- The vertical height is reduced to correct the aspect ratio and adjustable (VR1).
- The picture phase (horizontal position) is corrected (R13).
- Pin 2 from the existing monitor cable is coupled to the color 6 fix circuit by one of the Photomos relays IC3 pin 5 & 6.

If the monitor is instructed to go back into the CGA mode by detecting a positive going vertical sync pulse, then the output of gate C pin 10 falls low. The sequence of events is reversed but last before first. When pin10 falls low then C6 is rapidly discharged via R11 and D5. This causes initially the original 0.018uF tuning capacitor, (C419) to be switched back into the circuit. This protects the horizontal output stage (see section 5). Also at the same time the width control is un-shortened as M5 turns off.

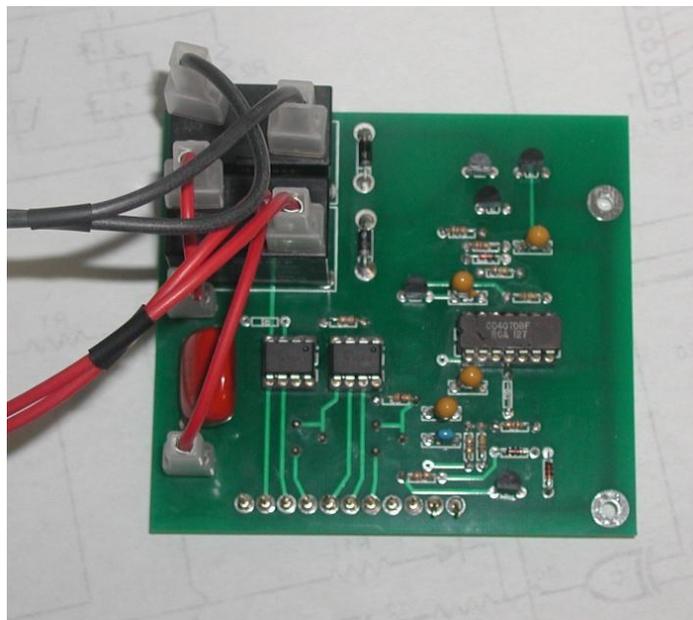
Shortly later R10 discharges C5 and M2 turns off, thereby returning the H scan frequency to 15.750 kHz and the vertical height to its normal value as set by the height control on the rear of the monitor.

Potentiometer VR2 allows adjustment of the H hold and to an extent the “phasing” of position of the EGA image horizontally on the screen.

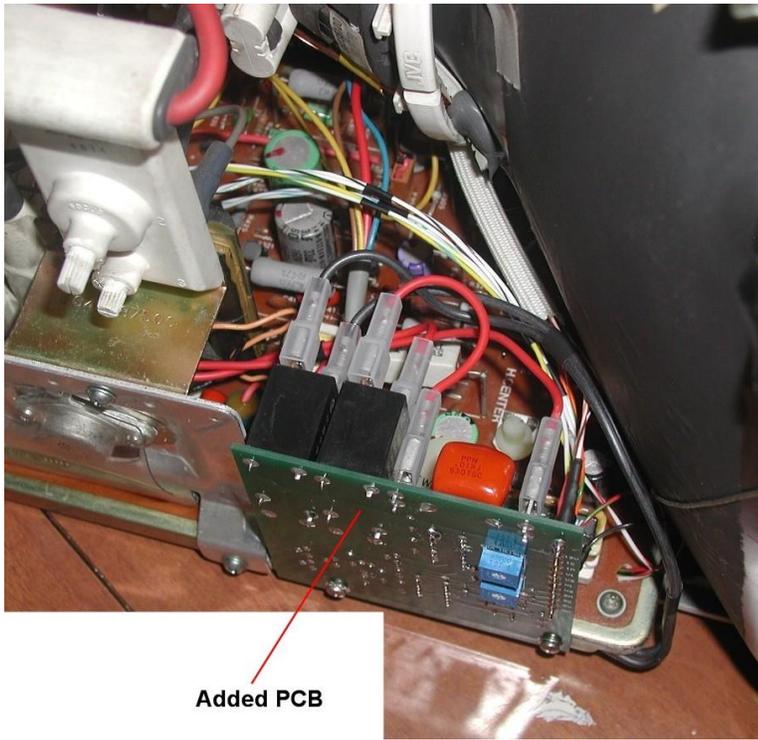
VR1 allows the correct height setting in EGA mode.

The best way to accurately set VR1 is to set the picture height initially with the monitor’s rear vertical height control potentiometer in a BASIC program screen 8 (15.750 kHz mode) to display a *round* circle. Then set VR1 in BASIC screen 9 (640x350 21.85kHz EGA screen) to display a *round* circle.

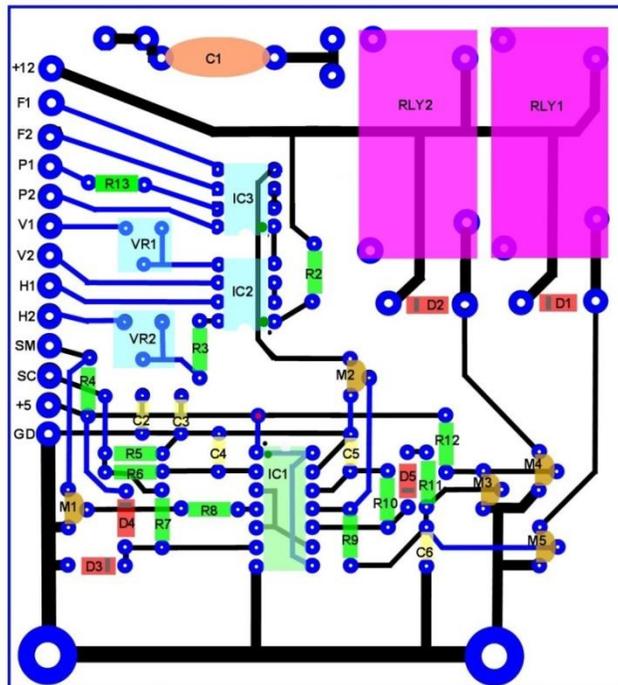
The photo below shows the pcb (a prototype version close not exactly the same as the final design:)



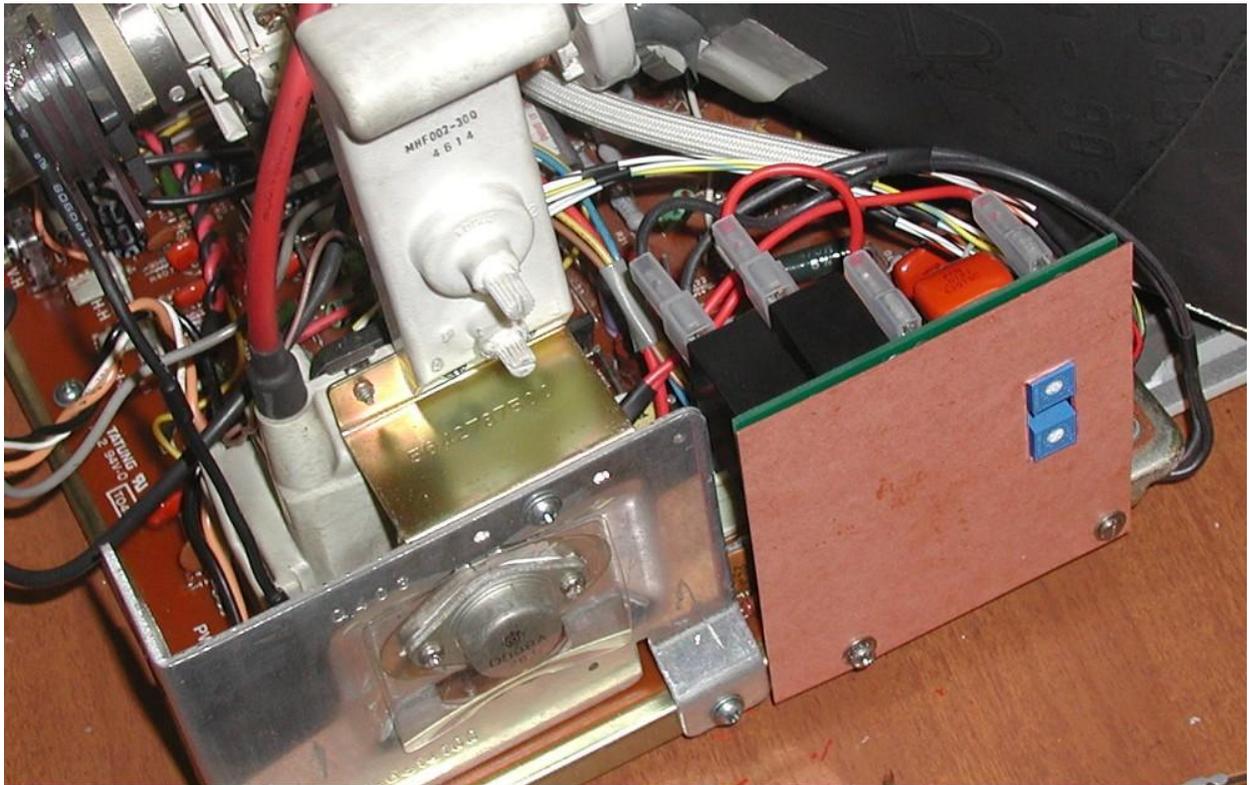
The photo below shows the pcb mounted in the 5153 on existing holes in the metalwork. The hole close to the front is easily tapped with a 4-40 UNC thread, and a screw and nut suffice for the other mounting which is a slot in the metal frame surrounding the monitor’s own pcb.



The photo below shows the actual pcb layout, looking from the side of the pcb that faces inwards to the monitor. The high scan rate (EGA) height control and (EGA) H hold control VR1 and VR2 face outwards for easy adjustment. The pcb is 92 x 83mm, the mounting holes 60mm apart and the one near the corner is spaced 5mm from each edge:



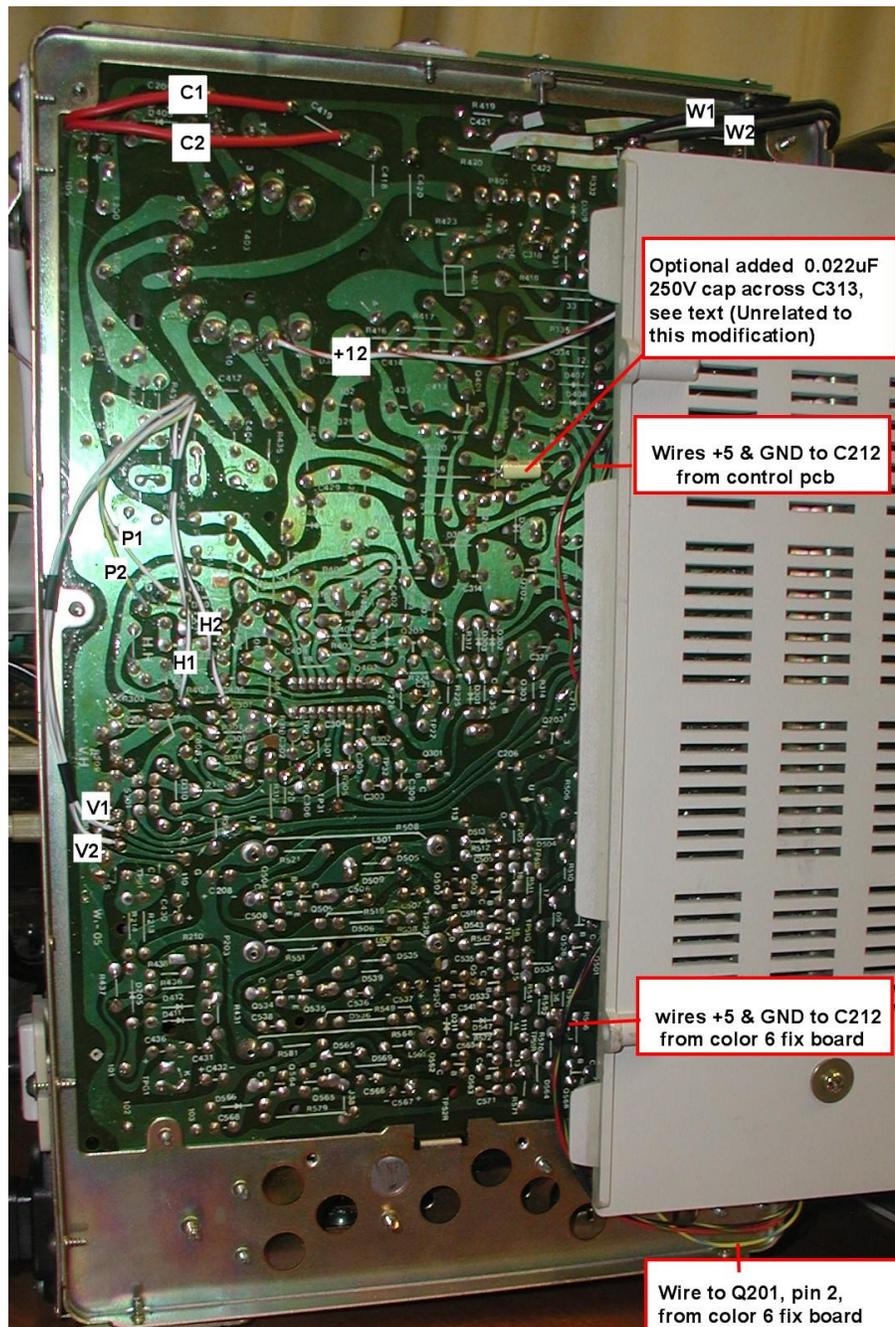
Since the pcb surface faces the inside of the cabinet area, although due to the cabinet taper at this point there is a good gap, it is worth putting some insulation over the pcb, much like IBM does for their CRT socket pcb assembly:



Where the connections go on the 5153's pcb :

The image below shows most of the connections. The SC (vertical sync from the cable) and SM (vertical sync to the monitor) pass across to the opposite side of the monitor where the pcb plug is that receives the monitor's connecting cable.

Since connections F1 and F2 (for the color 6 fix) also pass to the opposite side of the monitor, then these 4 wires can pass in a section of hollow sleeving just under the CRT bulb to the opposite side to near the monitor's cable connector area.



There is a phase error in EGA mode (horizontal picture position offset) that is corrected for by the connections P1 and P2. (see section 6 on how to accurately set set H hold and H phase pots on the main monitor pcb first). This is not often done correctly and the controls H.Hold and H.Phase interact.

W1 and W2 connect across the width coil (gain maximum width on EGA mode)

V1 and V2 connect across the vertical height pot (to adjust the EGA height).

H1 and H2 connect across R407 (To increase the H scan rate to 21.85kHz in EGA mode).

C1 and C2 connect from relay 2 and C2 (0.018uF) on the added pcb across the connections to C419.

The +12V supply for the control pcb is connected to pin 11 of the Horizontal output transformer (to gain a 12V supply).

(The added 0.022uF 250V yellow capacitor seen in the photo on the rear of the monitor pcb is nothing to do with this modification. It is the subject of a separate article to address a minor vertical scan linearity issue)

The yellow/blue wire is the wire that leads from the color 6 correction pcb (seen in the bottom right hand corner of the above photo) along with the two wires (from the +5V supply) that supply +5V power to the color correction pcb.(This yellow/blue wire turns on the Green channel for the color 6 fix, see below)

FIVE minor modifications are required to the 5153 monitor pcb and reasons are as follows:

- 1) C419 (0.018uF 630V polyester cap) is removed (but kept to fit to the control pcb as part number C1).
- 2) C419 is replaced with a 0.001uF 2kV rated polyester capacitor (Shortens flyback time in EGA mode).
- 3) C420 (0.015uF 630V) is removed and replaced with a 0.01uF 1000V rated polyester capacitor (assists in maintaining a satisfactory horizontal blanking signal in EGA mode).
- 4) Resistor R322 (4.7 ohms) is replaced with a 5.1 ohm $\frac{1}{4}$ w resistor (assists in the height adjustment range in EGA mode).
- 5) Capacitor C301 is removed and discarded. This part was a remnant of a system of combined H & V syncs and sync separation when the HA11235 IC was used for

domestic television sets where the V sync still had a small H component after the sync separator. With totally separate H and V syncs (from a computer) it is not required. In this case it causes a small vertical sync delay (vertical picture signal relative advancement with respect to sync) that shows up in EGA mode. So its best removed.

SECTION 3:

Correcting Color 6 with a “color 6 fix” pcb:

Since in the EGA system there are three R,G & B most significant bits (MSB) and three r, g and b least significant bits (LSB) color signals and the fact that the standard 5153 monitor cable has no pin 7 on its plug or cable connection for the b (LSB) then it would require a new plug & cable and some additional color mixing circuits into the R,G and B amplifiers in the 5153 to display the full EGA color set, including the LSB's.

However, the three R,G,& B (MSB) signals and the g(Intensity) signal are more than enough to create an excellent 15 color EGA image.

Without using the r and b LSB signals of the EGA system, then out of 16 possible colors (the usual 8 and their other 8 intensified counterparts) only color 6 is abnormal. Yet luckily IBM did provide the red LSB signal in the cable to the 5153, as mentioned they grounded that cable line at the pcb connector.

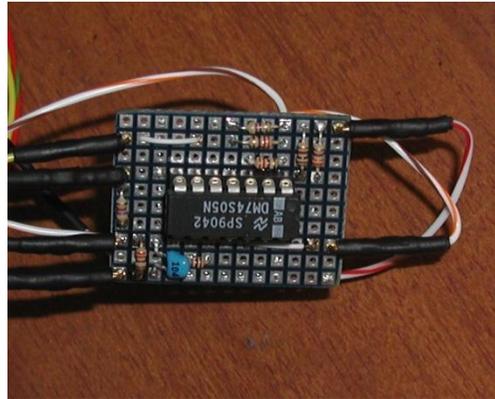
In summary in the EGA system, there are 6 (bits) color control lines: rgb,RGB. In CGA there are 4 control bits: I,RGB and the “I” signal line is common with the g LSB signal line of the EGA system.

The EGA 6 bit signal for the color Brown (color 6) the lines are logic level 010,100. This is a mix of R MSB and the g LSB. However, in the I,RGB system of the 5153 color monitor, Brown is 0,110 where the I signal is low, R & G are both logic high (giving low intensity yellow) and the 5153 monitor detects this state and lowers the green level in the gun amplifier system to display “Brown” instead of yellow.

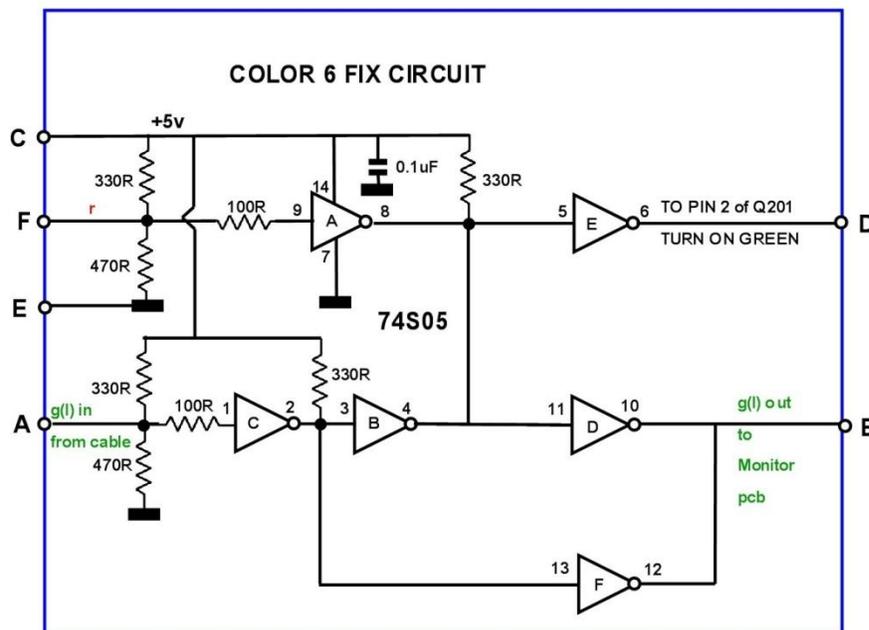
The above means that a Brown signal (color 6 in of an EGA color system) is displayed as intensified Red by a CGA “I,RGB” style color processing system. While all the other colors of the 0 to 15 set will display correctly using just the four I,R,G,B lines.

This *color 6 anomaly* can be corrected by using the r LSB signal (which is available at the cable inside the 5153) along with the g LSB signal to deactivate the intensification “I” and add Green. This ensures the 5153 monitor “sees” low intensity Yellow” or 0,110 and displays Brown correctly when presented with an EGA 010,100 Brown signal.

In a way this solution is taking a leaf out of IBM's books, where they modified a single color at the hardware level to create the Brown. The small sub circuit which achieves this is shown below:



This small color 6 Fix board is simply placed near the cable connector inside some large heat-shrink sleeve and suspended by its own connecting wires. The schematic is shown below:



How it works:

Due to the fact that the inverter gates are open collector types, two can be wired with their outputs tied together to make a two input NOR gate. Gates A and B are like this as are gates D and F.

A NOR gate behaves as AND gate with negated or true negative inputs (De Morgan's Theorem). Therefore, under the circumstance where the r LSB is low, and the g (I) signal is high (making pin 2 of gate C low) then pin 4 of gate B (and pin 8 of gate A) are high. This detects (partially decodes) EGA's 010,100 Brown signal. Therefore pin 6 of gate E falls low and this switches on the Green channel by grounding pin 2 of Q201 in the monitor's color process circuitry. Also Pin 10 of gate D is low, switching off the "I" signal. So the 5153's monitor's color processing circuit sees I=0, R=1 G=1 and displays Brown correctly.

For the intensified 8 colors in the EGA system, the drive signals are 111,RGB and since the r LSB is now high, for each of those colors, the circuit above results in the g(I) signal effectively passing through and no other changes.

Obviously without using the b LSB signal and with the above system, other EGA colors outside the basic set of 16, would display incorrectly.

(Notice how the logic looks odd in that gate F seems to bypass gate C and B. This is because these gates are open collector types and their outputs can be mixed in ways not possible with totem pole output gates)

Also the pull up resistor for gate D and F are resistors already present on the monitor pcb at the "I" input connection.

SECTION 4

Results and screen photos of 16 color EGA images on the 5153:

Photographing images on CRT faces can give some interesting problems, such as patterning and moiré effects. Also there can be a grey looking wide horizontal bar sometimes drifting vertically across the image. Also some of the images are a bit over exposed.

Firstly a small program was written in the BASIC graphics screen 9 which is a 640 x 350 EGA screen. To display 16 boxes of color, the first 8 regular colors and then 8

intensified ones, a bit like the CGACAL image. Also some circles were plotted and a white border added, to show how many pixels are visible at the perimeter of the display.

Due to some limitations of slightly longer horizontal fly-back time (6.7uS with this modification and a slightly longer vertical fly-back time than standard EGA) one vertical pixel row is lost at the image top. The horizontal fly-back was shortened as much as possible within limitations of the system (see section 5), and there are two pixels missing down the left hand edge. For example, in the test image below, the box around the perimeter of the image was plotted with the BASIC command:

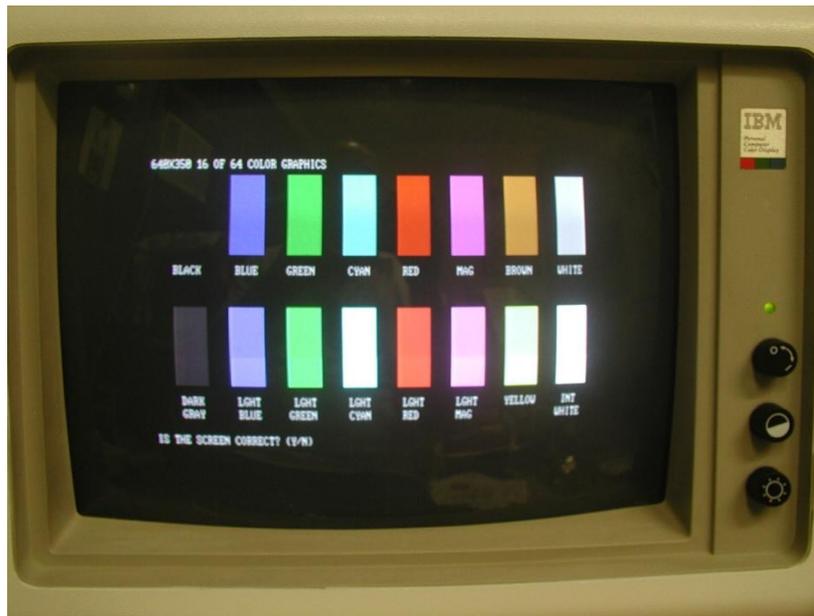
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LINE (0,1)-(637,349),15,B
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In other words pixels 638 and 639 on the horizontal and pixel 1 on the vertical are absorbed into slightly longer than standard EGA blanking times.

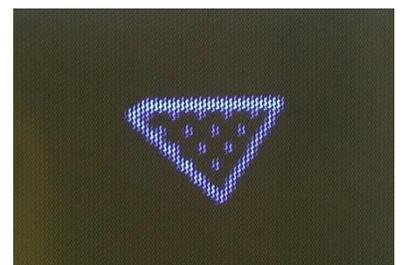
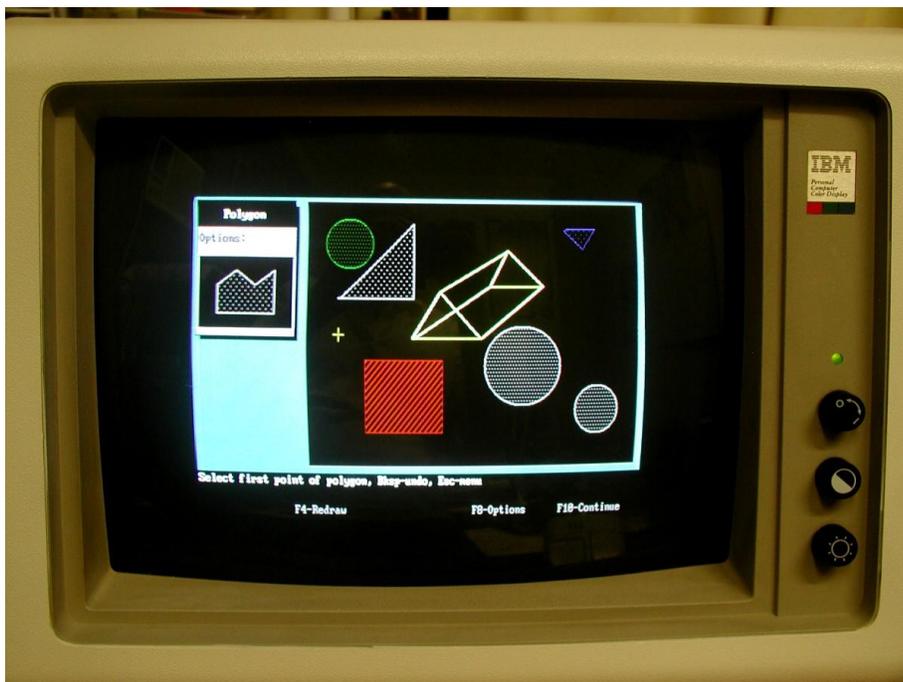


Notice there is a mild degree of Barrel Distortion of the image. The Pincushion correction circuit is a little over zealous running in the high scan rate mode.

The following photo is of the video test screen from the DIAG program that comes with the Video-7 EGA card, the photo is a bit over exposed, all of the 16 colors are correct:



The image below is some doodling in the program Draw Partner (this program is supplied with Harvard Graphics). Of interest is the ability to display very fine picture detail. One of the images is just a blue signal, so there are no convergence or beam registration issues for one color. The fine detail (excellent video high frequency response) is evident from the close up view of this part of the screen:



SECTION 5:

Scanning & flyback technical issues and Captain Nero's Red Matter:

IBM in their wisdom, for the 5154 dual standard monitor, had the insight to separate the generation of EHT voltage for the CRT final anode, from the horizontal scanning circuit. Why this was done will be clear with the information below.

Normally, for the average CRT computer monitor or TV set, the EHT voltage is derived from the horizontal output transformer during the fly-back time. This is because the peak voltage of the fly-back pulse is relatively large and easily transformed upwards and/or voltage multiplied upwards to a value of over 20kV to run the color CRT's final anode.

The fly-back pulse itself results from the horizontal output transistor being switched out of conduction at the end of the horizontal scan (crt beam on the right hand side of the screen) and then the magnetic field of the yoke and horizontal output transformer collapses. Since the circuit capacitance "tunes" the inductance of the horizontal yoke coils and horizontal output transformer, the field collapse is controlled as the two elements of inductance and capacitance form a resonant circuit. The "tuning" capacitance itself takes the form of the self capacitance of the horizontal output transformer and yoke plus additional tuning capacitance (the dominant value) connected across the output transistor's collector and emitter circuit.

As the magnetic field collapses, the stored magnetic energy is imparted to the electric field energy of the total capacitance or "tuning capacitance" that tunes the total inductance of the horizontal yoke coils and the horizontal output transformer. This stored energy peaks in the capacitance, as a voltage peak, about half way through the horizontal fly-back time (a quarter of a cycle of oscillation of the LC network).

This energy is later given back to the inductance of the yoke and transformer by the capacitance at the end of the fly-back time (crt beam now on the left hand side of the screen). At that point, the horizontal output transistor's collector voltage attempts to go negative, therefore the damper diode conducts. The 2SD898B horizontal output transistor in the 5153 monitor has the damper diode inside it, connected across the transistor's collector and emitter.

The magnetic field energy in the total inductance after fly-back is then *returned to the power supply* in a linear decaying manner to scan the left side of the CRT's screen. This is why the damper diode is sometimes called the "efficiency diode" as it returns energy to the power supply during part of the scanning cycle.

Because the horizontal yoke and transformer, as a load, is a substantially reactive load at its operating frequency, with minimal DC resistances, it was realized many years ago,

that if an energy recovery diode was deployed, that a *Horizontal* scanning system could be very efficient, much like an oscillator only requiring the injection of energy to overcome mainly resistive losses in the process.

An aside: The above principles do not apply to vertical scanning systems. A much higher yoke inductance required for the lower operating frequency and it has significant DC resistance is associated with that. Vertical output stages operate on a different principle as the vertical yoke, as a load, is substantially both resistive and inductive. Vertical scan output stages therefore do not have damper diodes and the output amplifiers driving them are basically linear (rather than switching amplifiers as in H output stages). Vertical output stages tend to resemble Audio power amplifiers for this reason and the drive voltage waveform to the yoke tends to be trapezoidal in character, rather than a rectangular voltage seen in Horizontal scanning systems. In horizontal scanning systems, the output device (transistor) is operating in a saturated switching mode, the transistor's drive waveform has little effect on scan linearity. Therefore linearity controls in the H scan system take the form of magnetic saturable inductors in series with the yoke and S correction capacitors. However in Vertical scanning systems the shape of the drive waveform from the output stage to the yoke affects the scan linearity so it is easy to have potentiometers and R-C networks in the Vertical amplifier system to control the vertical scan linearity.

There is some self capacitance of the yoke, the horizontal output transformer and also of the output transistor itself, but this total is unlikely to exceed 0.001uF. Most of the capacitance C controlling the fly-back time and fly-back voltage peak, is the added tuning capacitance. In the IBM 5153 they use three capacitors in series (two 0.018uF and one 0.015uF capacitors) as the "tuning capacitance". This distributes the high voltage across each 630V rated capacitor to reduce the chance of failure since the peak collector voltage on the 2SD898B (and voltage across these capacitors) is about 1100v.

Also the voltage across one of the capacitors that forms the tuning capacitance (C420) is tapped off to generate a signal for horizontal retrace blanking. It is necessary to blank the CRT's beam current during both the vertical and horizontal retrace (fly-back) times to avoid the beam illuminating the CRT screen at these times. In the 5153 monitor both the H & V blanking signals are passed on to transistor Q202.

Q202 introduces a rectangular wave into the R,G and B amplifier systems and this is AC coupled and then DC restored after the video output amplifiers by the diodes DS67,DS07 and DS37 to a fixed DC level set by the R,G & B background controls. This arrangement sets up a scenario where the signals driving the CRT's cathodes are set to a fixed reference level and the blanking periods drive the CRT's cathodes positive into beam cut-off.

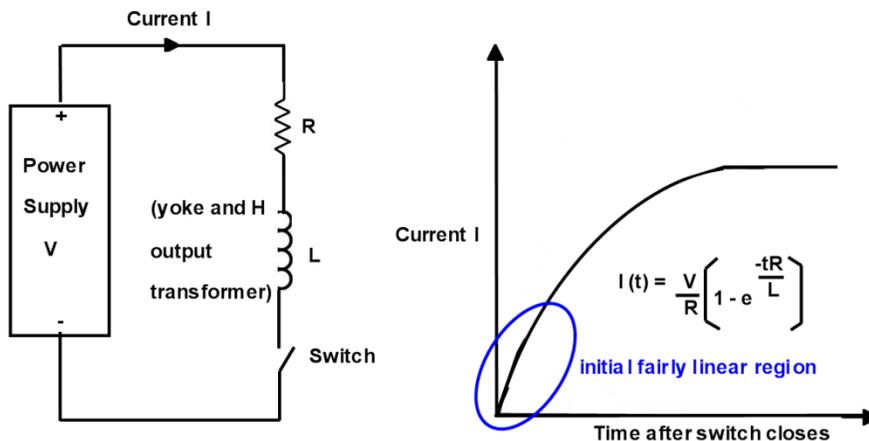
Since the tuning capacitance and inductance of the yoke and horizontal output transformer form a resonant circuit, the frequency of oscillation during fly-back and therefore the fly-back time depends on the tuning capacitor value (Since the values of the yoke and transformer are fixed and cannot be easily altered).

Both the deflection yoke (horizontal coils) and the horizontal output transformer are directly linked in most CRT based monitors. This means changes in either the scanning raster *width*, or the horizontal *fly-back time* (through alterations in value of the tuning capacitor) both affect not only the peak voltage (fly-back pulse amplitude) on the collector of the horizontal output transistor, but also the EHT voltage supplying the CRT's final anode.

In the 15.75 kHz scan mode (a frequency typical of the 5153 color monitor and NTSC standard TV monitors) the horizontal fly-back time is in the order of 10 to 11uS and the beam trace or scan time is in the order of 52 to 53uS. In the 21.85 kHz mode of EGA ideally the fly-back time is in the order of 5 to 6uS and the scan time around 39 to 40 uS.

The following diagram shows initially during scan time, during the right hand half of the picture scan, a linear horizontal scan current is generated:

For any Yoke and Horizontal output transformer combination and power supply voltage the slope of the current rise is fixed:



$$\text{Initial I rate of change of current} = \frac{dI}{dt} = \frac{V}{L}$$

The initial rise in current is fairly linear. Later it has the proportions of a typical inverted exponential wave. The proportions of inductance of the yoke and horizontal output transformer and supply voltage are chosen for a horizontal scan system so that the horizontal scanning circuit operates over this fairly linear region to attempt to obtain a linear scanning current for the deflection yoke because a linear electron beam scan is required.

Differentiating the equation for the graph above, shows that the initial current rise, or rate of change of current with time, or slope, has a value of V/L .

For any fixed power supply voltage V , and fixed inductance of some particular deflection yoke and horizontal transformer assembly L , the slope, or rise in scanning current with time is a fixed value of V/L .

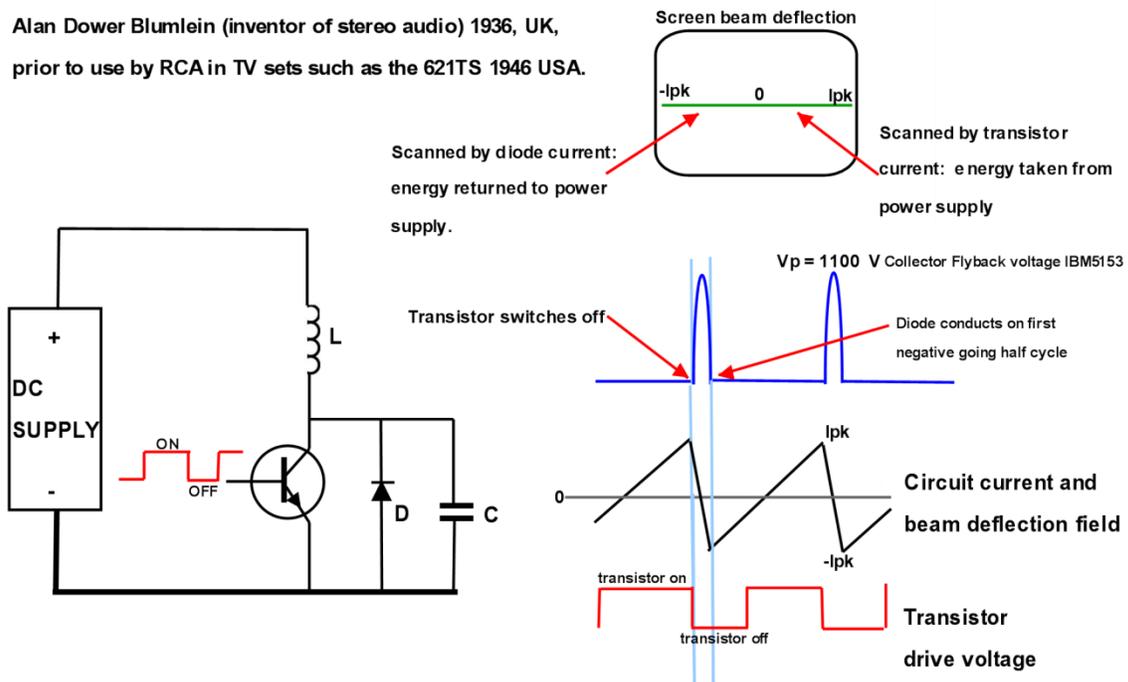
(The implications of this when altering the horizontal frequency are discussed below)

The diagram below shows a typical horizontal output stage, where C represents the total tuning capacitance, L the inductance of the yoke and horizontal output transformer and D the damper diode:

PRINCIPLES OF MAGNETIC HORIZONTAL DEFLECTION WITH ENERGY

RECOVERY (DAMPER) DIODE. First postulated (using tubes) by

Alan Dower Blumlein (inventor of stereo audio) 1936, UK,
prior to use by RCA in TV sets such as the 621TS 1946 USA.

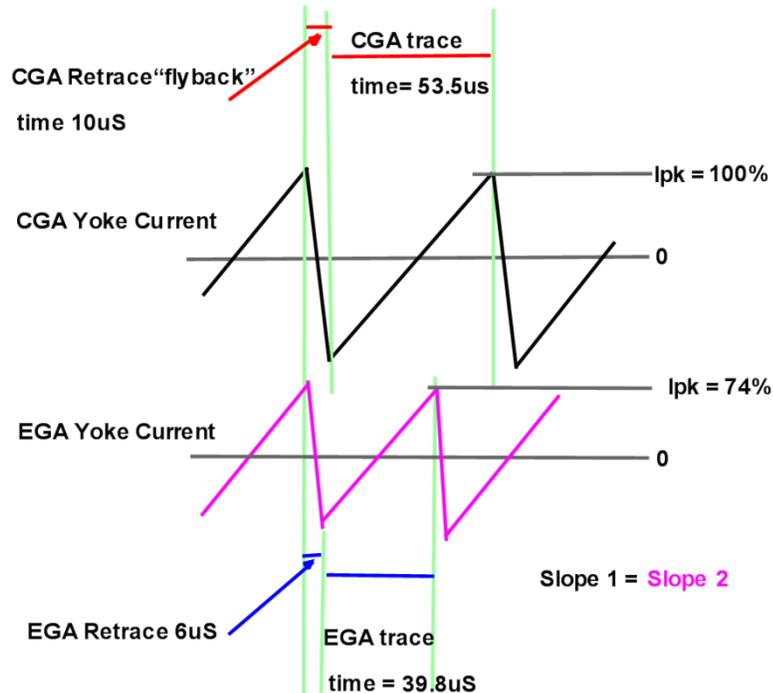


As noted this fundamental design with an energy recovery diode was invented using tubes in 1936 by Mr. Blumlein. He was killed testing Radar equipment in the early 1940's and Winston Churchill described his death as a national tragedy. Pre WW2, the damper diode had not found its way into TV sets in the UK. However, by the post WW2 period the damper diode or efficiency diode or booster diode idea had found its way into TV sets in the USA such as the RCA 621TS model released in 1946.

(The tuning capacitance C could equally well be placed across the inductor L because the power supply is an effective short circuit for alternating currents)

Essentially the transistor's collector current scans the right hand side of the screen and the damped current the left. At the moment the transistor switches off, the start of horizontal fly-back begins and the voltage across the capacitor (composed of three series capacitors in the 5153) and on the 2SD898B transistor's collector peaks. This is a fairly high peak of 1100v in the 5153. (Other windings not shown on the transformer transform this peak up and rectify it for the EHT voltage for the CRT's final anode).

One consequence of statement in red above is the following graph and remark that relates to what happens when the horizontal oscillator in the 5153 is sped up to 21.85kHz for EGA mode:



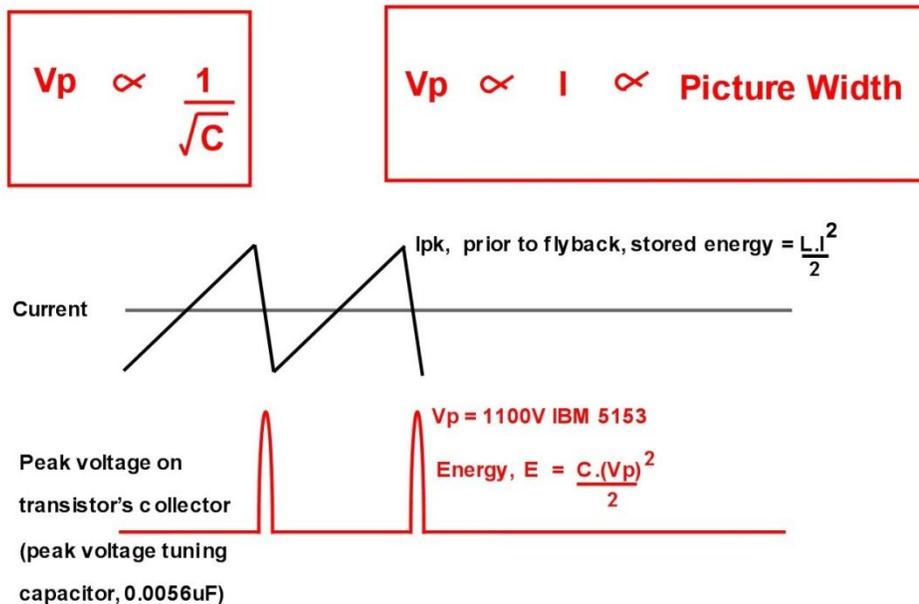
Since the rate of change of horizontal scanning current with time is fixed by the proportions of V/L , of the power supply voltage V and the horizontal output transformer and yoke inductance combination L , the shorter scanning time in EGA mode means that the peak horizontal yoke current I_{pk} , climbs to a smaller value of 74% in EGA vs 100% in CGA scan time.

This means the picture width in EGA mode (all other things unchanged except the horizontal oscillator frequency) is reduced to 74% of the CGA mode.

While the power supply voltage to the horizontal output stage could be increased by a factor of about 1.4 to compensate and gain more picture width, this is awkward and cannot be easily done due to another issue (see below). So the best method to help recover some picture width is to short out the width control, which is done by relay RLY 1 in the control pcb in the 21.85 kHz mode.

Since the peak current at the end of the scan (right hand side of the screen) represents the strength of the magnetic field and the stored magnetic energy, then a smaller width scan is a “lower energy” scan.

The energy imparted to the tuning capacitance, at the peak of the fly-back is therefore affected by the width of the scan. The actual peak voltage V_p generated on the capacitor during fly-back is dependent on the capacitor’s value too. As shown below the peak voltage on the tuning capacitor V_p is inversely proportional to the square root of the capacitor’s value and also proportional to the peak horizontal scan current and therefore the picture width:



The value of the three series tuning capacitors in the 5153 is about 0.0056uF and there will be some additional capacitance from the transistor and the transformer and yoke windings, probably in the order of about 0.006uF total.

Since the stored energy at the end of scan is proportional to the peak scan current (squared) and the energy when imparted to the capacitor (ignoring losses) is proportional to the capacitor's voltage peak voltage (squared), then the capacitor's peak voltage (or the peak fly-back voltage on the collector of the 2SD898B output transistor) is proportional to the picture width. As noted the width had dropped to 74% when the scan frequency gets increased to the EGA rate, but increased somewhat by shorting out the width control (lowering the yoke circuit inductance).

However the peak voltage developed across the capacitor is inversely proportional to the square root of the capacitance value. This leads to another remark:

Reducing the value of the tuning capacitance, to shorten the retrace or fly-back time, results in an increase in the capacitor's peak voltage during the fly-back time.

The fly-back time in the 5153 monitor as it is in CGA mode around 10uS to 11uS is too long for an EGA signal, ideally it needs to be around 6uS.

Replacing one of the 0.018uF capacitors, C419 with a 0.001uF capacitor reduces the fly-back time to around 6.7uS. This causes the peak collector voltage to climb to about 1300v (without zener clamping) when the monitor is running with the 21.85 kHz scan rate and lower energy (reduced width). The transistor is rated at 1500V.

If for any reason, with the lower tuning capacitor value present as operating in EGA mode, the scan rate accidentally went back to 15.750 kHz which has full picture width (higher energy) , the collector voltage would peak far too high. This would be "unthinkable" and be very destructive to the monitor and could cause very high EHT voltages, possibly X-ray emissions, destroy the horizontal output transistor and destroy the high voltage rectifier assembly in the H output transformer and probably cause a number of other component failures. For a CRT monitor this would be the equivalent of putting a drop of Captain Nero's Red Matter into its horizontal output stage (Of course this failure could also happen when existing tuning capacitors go open circuit, fortunately that is fairly rare).

The scenario painted above is best prevented in two ways, one an absolute protection and the other a relative protection. (We don't have the time travel options to go back

and prevent the disaster before it occurs, that were useful for Spock to defeat Nero in Star Trek).

Relative protection:

As noted the add on control pcb has been designed with time delays so that when switching into EGA mode the scan rate is altered to the higher value (low energy mode) before the larger tuning capacitance is switched out to shorten the fly back. In coming out of EGA mode, the tuning capacitance is switched back in first, before the scan rate is reduced and a full width (higher energy) scan is re-established.

Absolute protection:

To protect the output transistor a string of fourteen 75v 5W 1N5374B zener diodes are connected from the transistor's collector to ground. This limits the peak collector voltage to around 1200V and protects the transistor and limits any possible excessive increases in EHT. Testing the EHT shows it to be around 21kV in CGA mode and it increases to around 23kV in EGA mode.

The 14 diodes have their wires soldered together in series in the same direction with their cathodes (line on the diode body) pointing toward the transistor's collector. They are placed in sleeve and connected to the collector solder lug on the 2SD898B and the other end of the diode array connected to a screw lug on the opposite side of the monitor

In use the diodes are not conducting to any significant extent in CGA mode, and just snub off the top of the fly-back waveform in EGA mode.

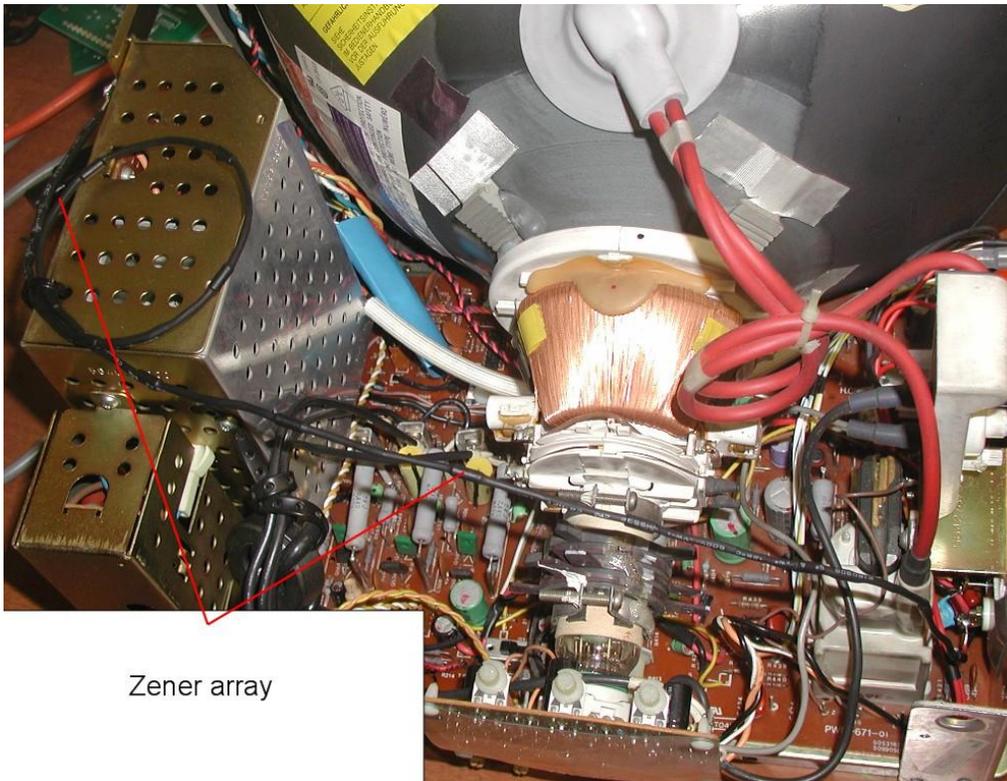
If it was attempted to gain more scan width, by increasing the power supply voltage powering the horizontal output stage as mentioned above, as a method of correcting for the width reduction in a "system of fixed inductances", then the clamped energy would be excessive in these zeners. Without them the horizontal output transistor would be at risk.

The photo below shows the 14 zeners in series before they were put in heat shrink sleeve.

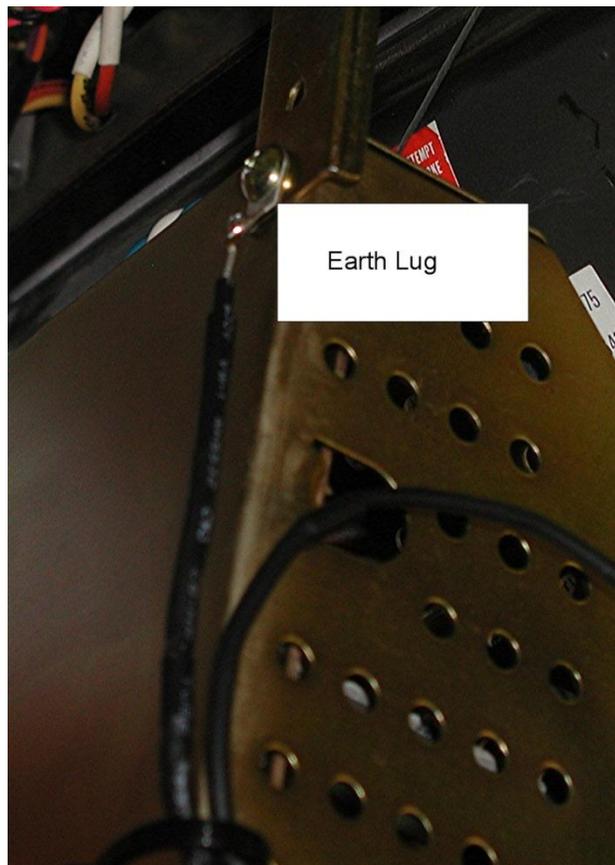


The main issue is to keep these away from most other components. In the EGA mode the diode string runs at about 80 degrees C. So they are best strung across the monitor to the other side to an earth lug.

When soldering to the 2SD898B's collector lug, make sure to loosen the collector lug mounting screw first and re-tighten in after the soldering has cooled down. This puts less stress on the 2SD898B's plastic mounting insulator under the lug.



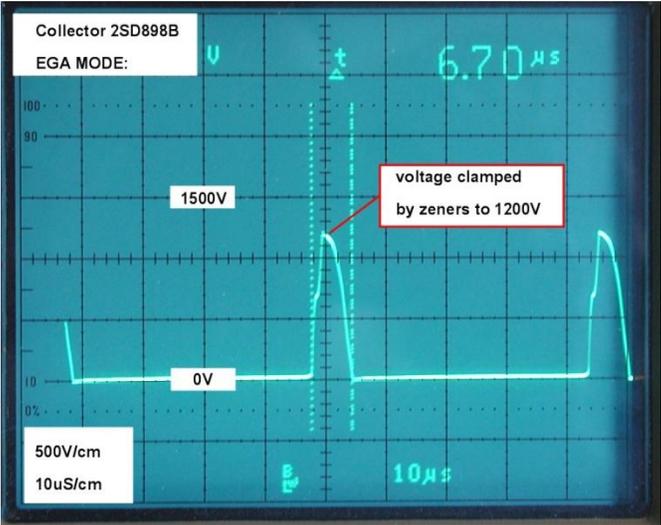
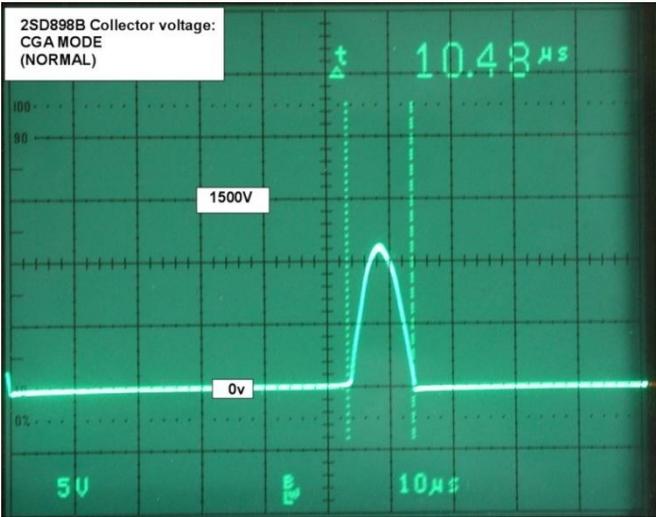
Zener array



Earth Lug

There is no single junction device that can serve the purpose of these 14 diodes. The dissipation is too high and the voltage too high for a *single junction* and power is better spread across 14 devices. One trick that has been tried for this sort of application is a zener diode from the collector to base of the output transistor; this turns the transistor into an “active clamp”. They do this for some car ignition coil driver transistors, but that puts most of the energy dissipation into the transistor’s junction which is less favorable. In this case due to the high repetition rate of the pulse clamping (unlike for an ignition system) this is not an option. The 1N5374B diodes are not expensive at around 30 cents each.

The recordings below show the collector voltage of the 2SD898B in the normal CGA mode, and in the EGA mode where the fly-back is shorter and the peak voltage is higher, the zeners are just clipping the top of the fly-back peak. The fly-back time is shortened to 6.7uS:

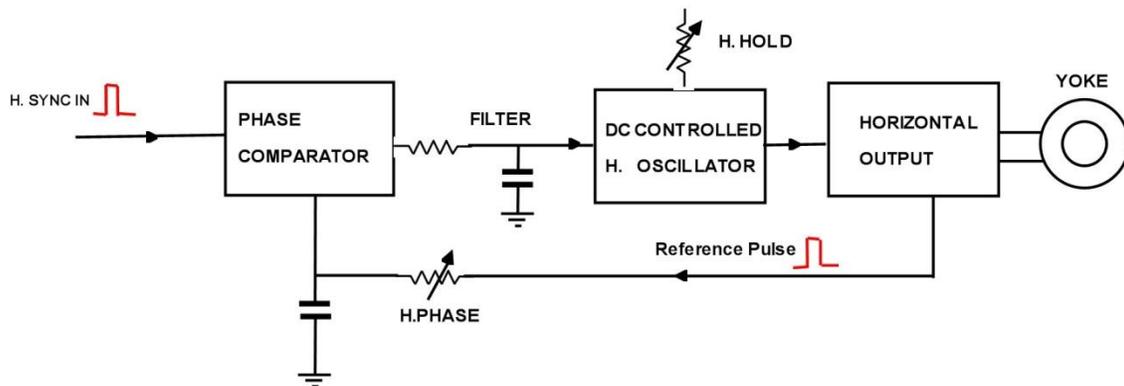


SECTION 6:

How to correctly set the 5153 monitor's own H.Hold and H.Phase controls:

Most cathode ray tube TV sets of the late 1930's and immediate post war period simply injected the horizontal sync pulse into the horizontal oscillator (typically a blocking oscillator) so the horizontal stage was synchronized per Line, much like the vertical stage being synchronized per Field or frame. However if a noise pulse came along this would cause a "line tearing" effect. So ultimately it was realized that it would be better to have a phase locked loop for horizontal scan synchronization for a TV set or VDU. In this scenario the H oscillator is a voltage controlled (VCO) or DC controlled oscillator. The phase of the incoming sync pulse is compared to the horizontal oscillator phase (although the reference pulse is normally taken from the H output transformer). A filtered "error voltage" is produced and used to control the H oscillator frequency around some center value:

**BASIC ARRANGEMENT HORIZONTAL HOLD.
(A PHASE LOCKED LOOP WITH A CAPTURE RANGE)**



Since the circuit is fundamentally a PLL (phased lock loop) any noise pulses in the H sync pulses are averaged out by the filtering and the horizontal oscillator cannot abruptly respond to sync pulse noise and the line tearing effect eliminated.

One result of this design is that the circuit has a "capture range" meaning a dynamic range where the filtered control voltage from the phase detector controlling the H oscillator frequency, corrects for any offset (such as the H.Hold potentiometer) or any oscillator drift due to component heating attempting to force the average oscillator

frequency up and down. The result of this is that when the H.Hold control is adjusted, the horizontal synchronization remains “in lock” with the H sync pulse and will appear to suddenly lose horizontal lock at either end of the control’s range (typically)...but in any set the control range might not extend each way far enough to drop it out of lock on each side, so as to be able to find the middle of that control range.

As the H oscillator’s average frequency is attempted to be forced up and down by the manual H. Hold control, the phase of the sync pulse, relative to the actual scan (the reference pulse) shifts with a bigger or smaller time delay between the two pulses. This effect shifts the relationship of the picture information in the video signal with respect to the actual horizontal scan requiring higher or lower corrections to the H.Phase control to horizontally center the image on the scanning raster.

Therefore as the H.Hold or the H.Phase control is rotated the picture shifts right and left horizontally. So it turns out there are a number of positions(combinations) of both the H.Hold control and the H. Phase control position where the picture is in lock and also has the correct positioning of the picture information on the screen.

If for example the H hold potentiometer is set closer to one extreme (but still in picture lock) and the phase control is adjusted to compensate the image shift and centre the video image horizontally this is not ideal, as it is relying on a larger correction from the PLL system to provide a larger offset correction to the horizontal oscillator frequency.

If the H .Hold control is nearer one extreme the H oscillator could lose lock when the monitor was first turned on from cold. This is because this type of PLL system tends to have a wider tolerable offset range while in lock, but a narrower capture range when out of lock.

Ideally, the horizontal oscillator frequency is set very close to the running frequency of 15.750 kHz with no +/- offset added from the PLL loop...meaning the output from the phase detector is in the centre of its dynamic range. In practice there is no quick way to know where this “control setting combination” is due to the capture range of the PLL circuit.

Fortunately, there is a way around this to get the close to ideal setting for the H.Hold and H.Phase control for minimal horizontal image drift:

Capacitor C213 couples the horizontal sync pulse into pin 16 and 17 of the HA11235 sync processor IC in the 5153. One end of this capacitor can be temporarily disconnected by removing the solder from the pcb pad with solder wick. Then the monitor’s H.Hold can be adjusted so that the free running H frequency matches the sync and video information for a typical CGA 15.750 kHz signal. The image may just barely lock due to stray sync pulse coupling of the circuit tracks around C213. Once that

is set the monitor's H.Hold control is left alone and the capacitor reconnected. Then to set the H.Phase control, display a Screen 8 basic image with the command:

```
LINE (0,0)-(639,199),15,B
```

This plots a white box outline. The monitor's H.Phase control is then turned to centre this box horizontally on the screen face. The monitor's H.Hold and H.Phase controls are now properly set and this should be done before the control board is added to the monitor. The values on the control board, including the correction to the H.Phase, have been chosen so that the EGA Hold control also doubles as the H phase control in the EGA mode. These steps are necessary because in EGA mode any H phase drift is more obvious due to the shorter blanking interval and active pixels extending over the full available scanning time. Therefore any H.Phase or horizontal picture drift is better minimized.

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